HIGH SPEED TDM RING NETWORK FOR BACKBONE LAN APPLICATIONS

by

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APRIL, 1989

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by
KRISHNA KUMAR P.

to the
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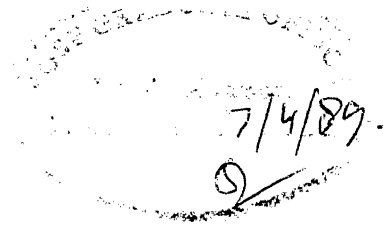

CERTIFICATE

This is to certify that the present work titled "High Speed TDM Ring Network for Backbone LAN Applications" by Mr.Krishna Kumar P.(Roll No. 8710432) has been carried out under our supervision and has not been submitted elsewhere for a degree.

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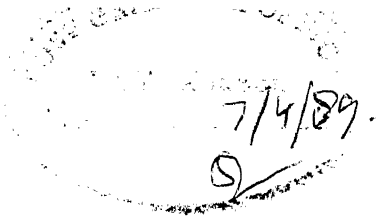

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Finally, I would like to express warm regards to my parents and my brother for their blessings and encouragement.

KRISHNA KUMAR P.

ABSTRACT

High speed Local Area Networks (LANs) are increasingly being used as backbone networks. Some of the recent developments in this area are networks with integrated service capabalities. After reviewing some recent developments in this subject, the advantage of a ring LAN topology, particularly for fiber optic LANs is pointed out.

Subsequently the design of a high speed, demand assigned, distributed control, synchronous, Time Division Multiple Access (TDMA) ring network suitable for integration of voice and data traffic has been carried out.

The feasibility of the network has been partially demonstrated by implementing a ring which supports two nodes.

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CHAPTER 1

INTRODUCTION

Computer terminals and peripherals are fast escaping from the computer center and are reaching out into offices and homes. These systems are being connected to local or wide area networks. Such linkage provides many services such as electronic mail, access to remote data bases and value added communication facilities.

With the introduction of digital techniques in telephony, switching, transmission and subscriber loops, public telephone networks are evolving into end to end digital networks capable of supporting voice and data services. This has led to the concept of Integrated Services Digital Network (ISDN) [1] offering access to a wide range of services over a single subscriber line. A comprehensive protocol set offering support to diverse data and circuit switched services are now available for ISDN.

Current LANs provide mainly data transfer oriented services. Of late many attempts have been made to provide voice and data on a single network. Hooper et. al.[2] provides a review of the Cambridge fast ring which is a slotted ring network capable of handling voice and data. Amada et. al.[3] propose a PABX based architecture for an integrated voice data system. Kamesh [4] has implemented a ring network suitable for voice data integration in a local area environment. The Fiber Distributed Data Interface [FDDI]

standard [5] for fiber optic networks includes provisions for voice data integration.

In this thesis, the design of a high speed TDMA based ring LAN which supports voice and data traffic and is suitable for fiber optic medium has been carried out.

1.1 INTEGRATED SERVICES LANs

Voice and data place differing requirements on the communication network which makes their integration on to a single network a difficult task. Voice can tolerate reasonable errors, but places stringent time constraints on the network. Voice prefers an end to end circuit switched network. Data on the other hand cannot tolerate errors but allows for random delays and permits the network to deliver them out of sequence. Further, data sources are mostly bursty in nature in contrast to voice sources. So a packet switched network is ideal for data traffic. Different techniques have been reported in literature to effectively integrate voice and data on a single network. A few of them are mentioned below.

In the 1970's the IEEE established committees to develop standards for LANs. These committees came up with the IEEE 802 LAN standards. The objective of IEEE 802 based LANs was to provide a high burst throughput for services such as file transfer or remote log in between computer systems. Attempts to provide voice service in these LANs have not proved cost effective [6,7]. Of these, the IEEE 802.5 (Token Passing Ring) seems to lend itself best for voice-data

integration, since it allows for time bound transmission of higher priority packets [5].

Several attempts have been made to provide integrated communication using PABXs. [3,8]. PABX oriented networks are well suited for voice switching, but have poor call set up times to provide satisfactory response for computer traffic which is predominantly bursty. Further, these networks are not suited for broadcast. Amada et. al. [3] use a PABX with a centralized high speed packet switch module to achieve voice data integration.

In slotted ring networks such as the Cambridge Fast Ring, bandwidth can be partitioned for use by different types of traffic. This is made possible by allowing different slot sizes. Maintaining synchronization of the ring becomes complex when such techniques are employed [9].

In TDMA based networks the slot size is made compatible to PCM voice traffic requirements thereby making voice data integration possible [4].

In FDDI [5] voice data integration is achieved by making a proper choice of the token rotation time. This technique is explained in detail in the next chapter.

1.2 FIBER OPTICS IN LANs

Optical fibers have a number of properties which make them natural candidates for high capacity transmission systems. The most important of these are:

(1) Large bandwidths capable of supporting data transmission rates of the order of 100 Mbps at relatively low costs.

(2) Immunity to electromagnetic interference.

(3) Extremely small physical dimensions.

(4) Low attenuation, typically a few decibels per kilometer.

Ring and star configurations lend themselves naturally to fiber optic implementation, since only point to point communication is required [10]. There are ring access protocols such as token passing with excellent throughputs even at high bandwidths [11].

Conventional data sources like a computer system cannot generate enough traffic to utilize the large bandwidths that fiber optic links provide. The cost of interfacing individual systems to the fiber optic link could prove prohibitive. So fiber optic networks are being envisaged as backbone networks to which many front end networks such as the popular IEEE 802 LANs are connected through bridges. (Fig.1.1). Backbone fiber optic networks with large bandwidths, with a span of several tens of kilometers can interconnect many individual networks, multiplexed voice traffic and large computers.

Many LANs using fiber optic medium have been reported in literature. A few of the important ones among them are mentioned below. The important features of these LANs are given in Table 1.1.

Network	Configu--ration	Data Rate	Media Access Protocol	Types of Traffic
Fibernet-II	Active Star	10 Mbps	Centralised CSMA/CD	Data only
D Net	Several	10 Mbps	Distributed Locomotive	Voice and Data
Express Net	Bus	10 Mbps	Attempt and Defer	Voice and Data
Hubnet	Dual Root--ed Tree	50 Mbps	CSMA with collision avoidance	Data only
ProNET-80	Star Conf--igured Ring	80 Mbps	Token Passing	Data only
FDDI	Ring	100 Mbps	Timed Token Passing	Voice and Data

TABLE 1.1 : Comparison of Fiber Optic LANs

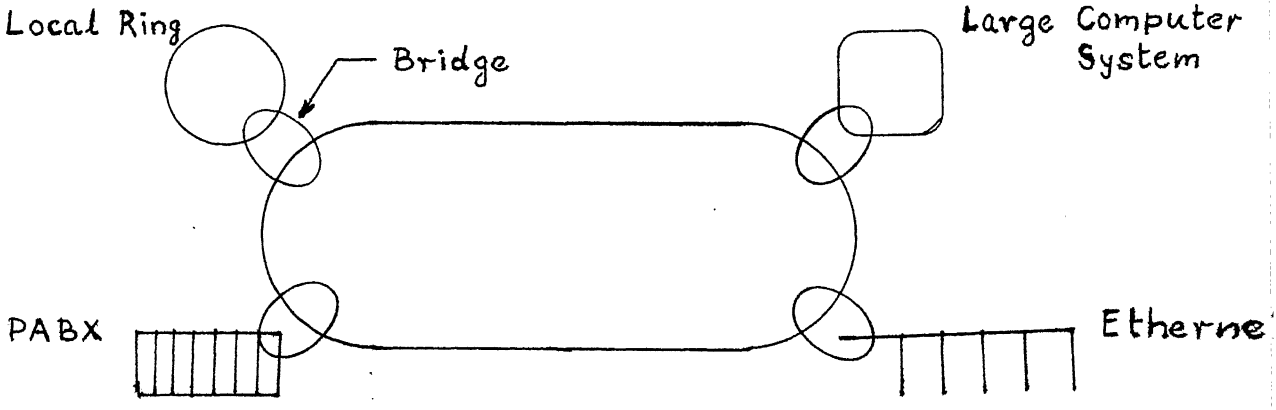


FIG. 1.1 BACKBONE NETWORK

Fibernet-II [12] is an active star configured fiber optic LAN which is plug compatible with IEEE 802.3 Ethernet at the transreceiver cable interface. The configuration of the network is shown in Fig. 1.2. The collision detection is implemented in the 25 port star repeater. The span of the network is 2.5 km. and it can support upto 1000 stations. The advantage of Fibernet-II is that it uses a fiber optic cable instead of the Ethernet coaxial cable.

The IEEE 802.3 CSMA\CD protocol reduces the throughput drastically at high data rates because it is sensitive to the end to end propagation delay of the network. Hubnet (Fig.1.3) [13] overcomes this deficiency of the Ethernet type networks. It is a 50 Mbps LAN using glass fiber as the transmission medium and uses a dual rooted tree structure with twin fiber communication paths. Hubnet uses a centralized selection-broadcast mechanism. It avoids collisions by blocking all other input lines when a station is transmitting and arbitrarily choosing one of them to transmit when several stations attempt simultaneously.

Expressnet Fig.1.4 [14] is configured as a unidirectional bus and uses a rather complicated `attempt and defer' protocol which enables it to carry data and voice at high efficiency on the same bus.

D Net [14] also uses a unidirectional bus as the transmission medium. Its configuration is shown in Fig.1.5. It can be reconfigured as a star or as an open ring also. It uses a simplified version of the Expressnet's access

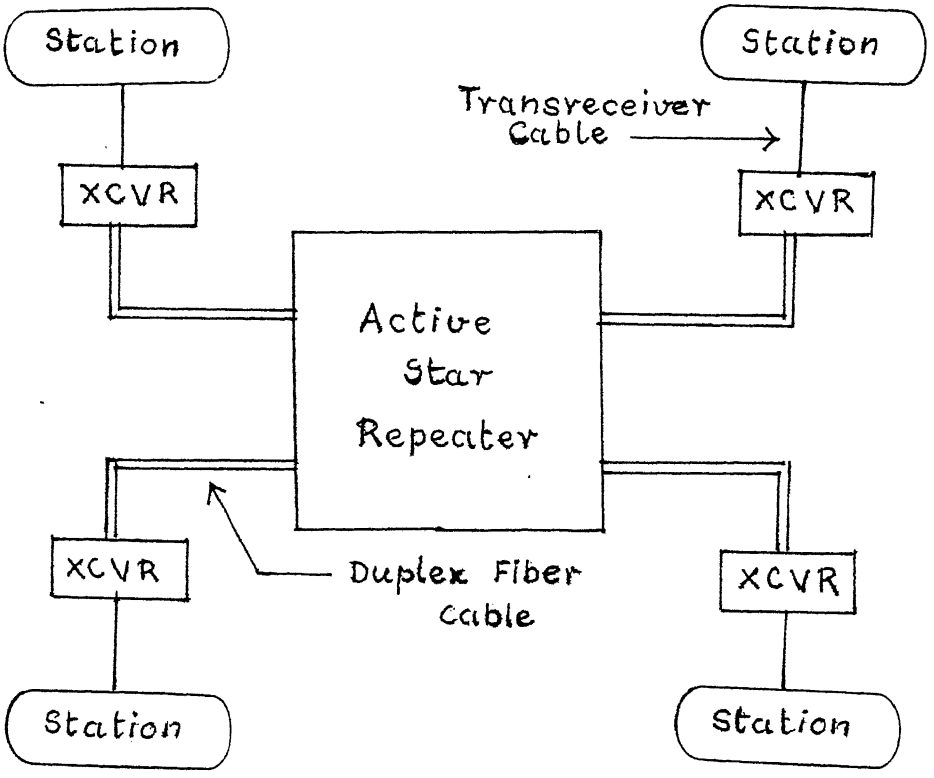


FIG. 1.2 CONFIGURATION OF FIBERNET II [12]

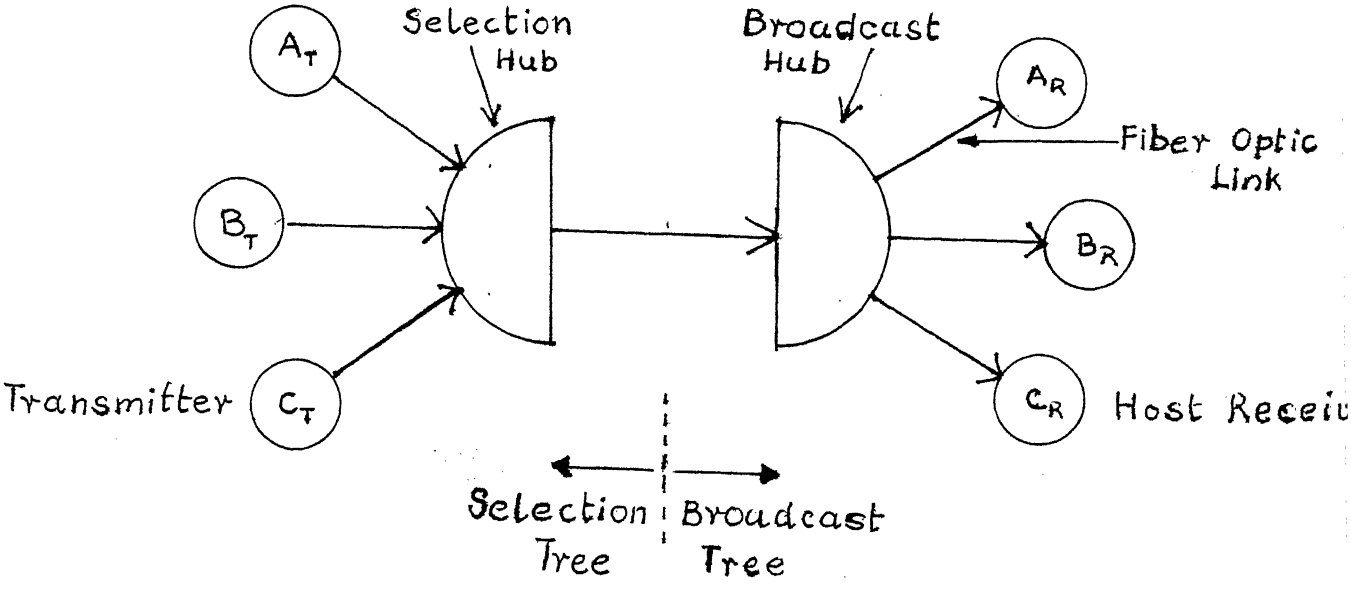


FIG. 1.3 CONFIGURATION OF HUBNET [13]

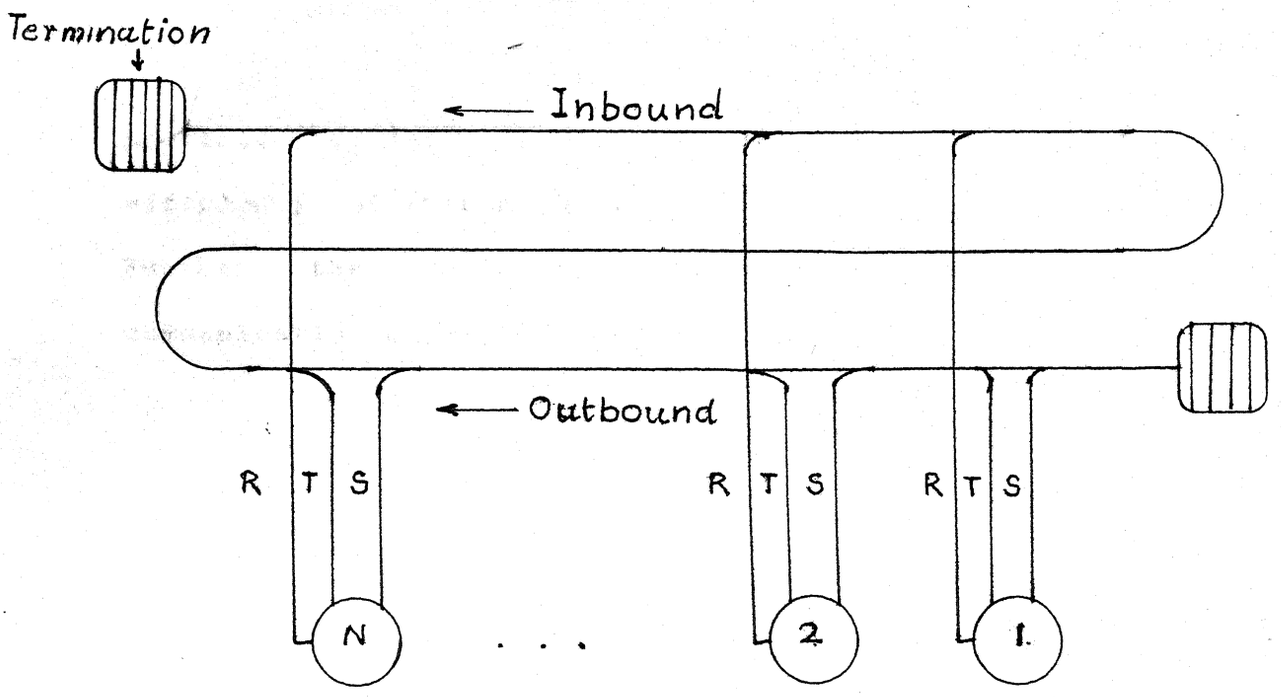


FIG. 1.4 CONFIGURATION OF EXPRESSNET [14]

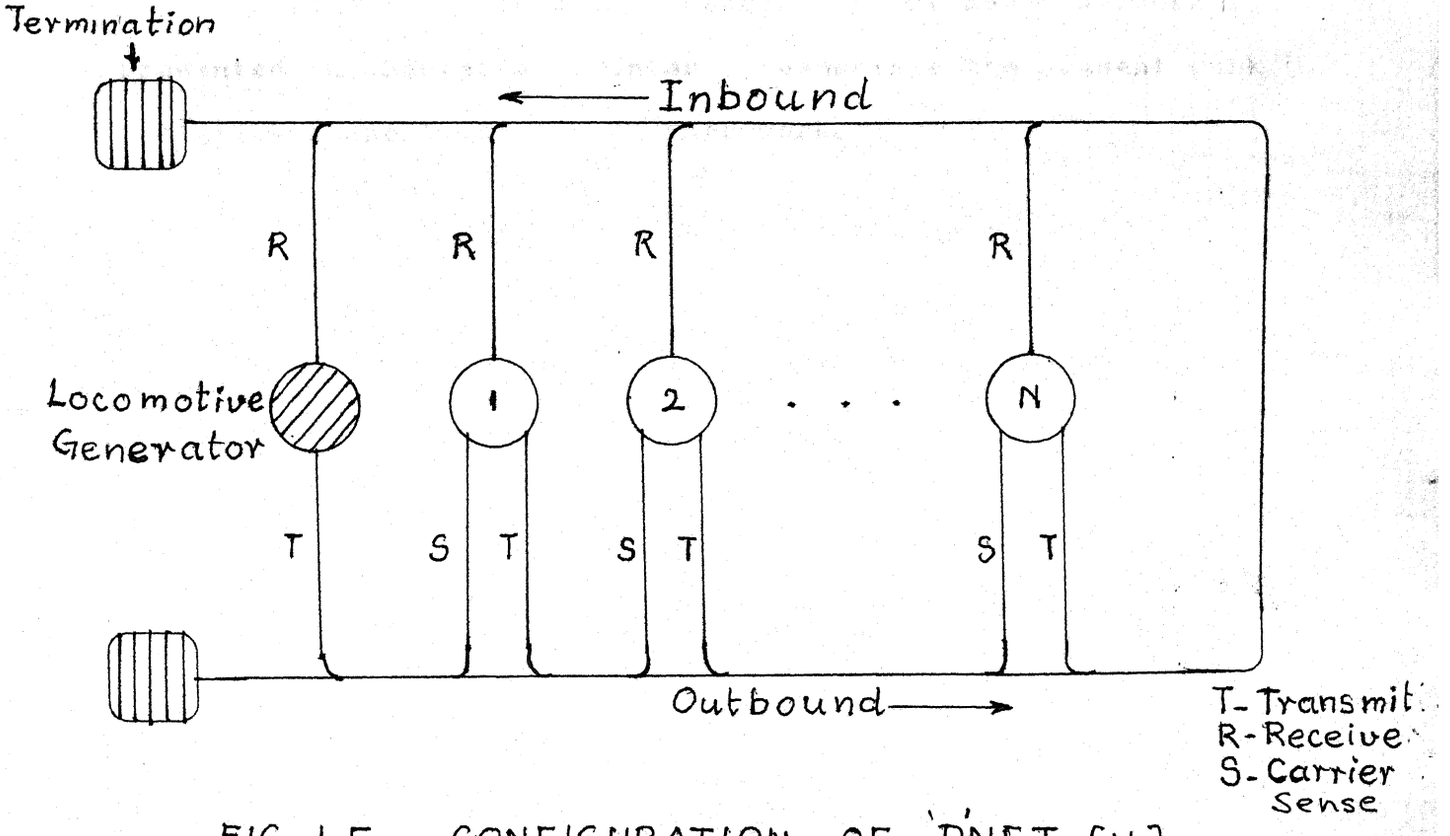


FIG. 1.5 CONFIGURATION OF 'DNET [14]

protocol called distributed locomotive protocol. The efficiency of this network is not limited by the data rate. Further, the low bounds on packet delays makes real time communication possible.

Several ring fiber optic LANs have been reported in literature.[3,4,15-19]. Some of them are discussed in the next chapter.

1.3 ORGANIZATION OF THE THESIS

Chapter 2 reviews some important backbone fiber optic ring networks reported in literature. The design of a high speed network that can carry data and real time traffic is carried out in chapter 3. The details of the hardware implementation of the node processor for the above network is presented in chapter 4. Chapter 5 summarizes the present work and gives suggestions for further work.

CHAPTER 2

BACKBONE FIBER OPTIC RING NETWORKS

In the previous chapter the suitability of a ring topology for high speed fiber optic networks was pointed out. In this chapter a few important backbone networks and fiber optic ring networks which support voice and data traffic are reviewed.

In section 2.1 some important backbone networks are discussed. An Integrated Voice-Data LAN is reviewed in section 2.2. Section 2.3 reviews a popular commercial backbone network named ProNET-80. In Section 2.4 some of the salient features of FDDI are pointed out.

2.1 BACKBONE NETWORKS

Several ring networks suitable for backbone network applications have been reported in literature. Of these, two recent networks which support both voice and data traffic are discussed below.

Kitayama et. al. [16] describe the details of implementation of a 32 Mbps token ring backbone network developed to interconnect sixty four 10 Mbps CSMA\CD subnetworks. For the token ring, FDDI access protocol has been employed. The subnetworks are connected to the backbone network through bridges. The backbone network can span 128 km. and the maximum separation between bridges is 2 km.. The configuration of the network is shown in Fig.2.1 and its

important features are tabulated in Table 2.1.

Tennenhouse et. al. [17] describe the architecture of a Unison Exchange which uses a Cambridge Fast Ring (CFR) to interconnect the distributed local networks. Cambridge rings and Ethernets are connected to the CFR through `portals'. Communication between peer portals is established through exchange of CFR slots. The exchange can be attached to links that conform to ISDN recommendations through a `Ramp' which is attached to the exchange CFR. The Unison exchange presents a high speed packet switched interface to the portals. The individual packets are small (256 bits) and so packetisation delays are minimal. Inter-site packets are carried over a dynamic circuit switched network in which both the bandwidth of the inter-site connections and their topology can be dynamically adjusted. The exchange structure is shown in Fig.2.2.

2.2 INTEGRATED VOICE-DATA LAN

Kamesh [3] has implemented an integrated voice-data LAN. It is a ring network based on subscriber access to a 64 Kbps slot, employing 16 slots per frame and using In Slot Signaling. Framing and synchronization are established by sending a unique pattern. Data is Manchester encoded before transmission. TDMA is the multi-access protocol used and the slots are assigned on demand. The network uses a fast circuit switched approach which has small call set up and relinquish times and provides high throughput.

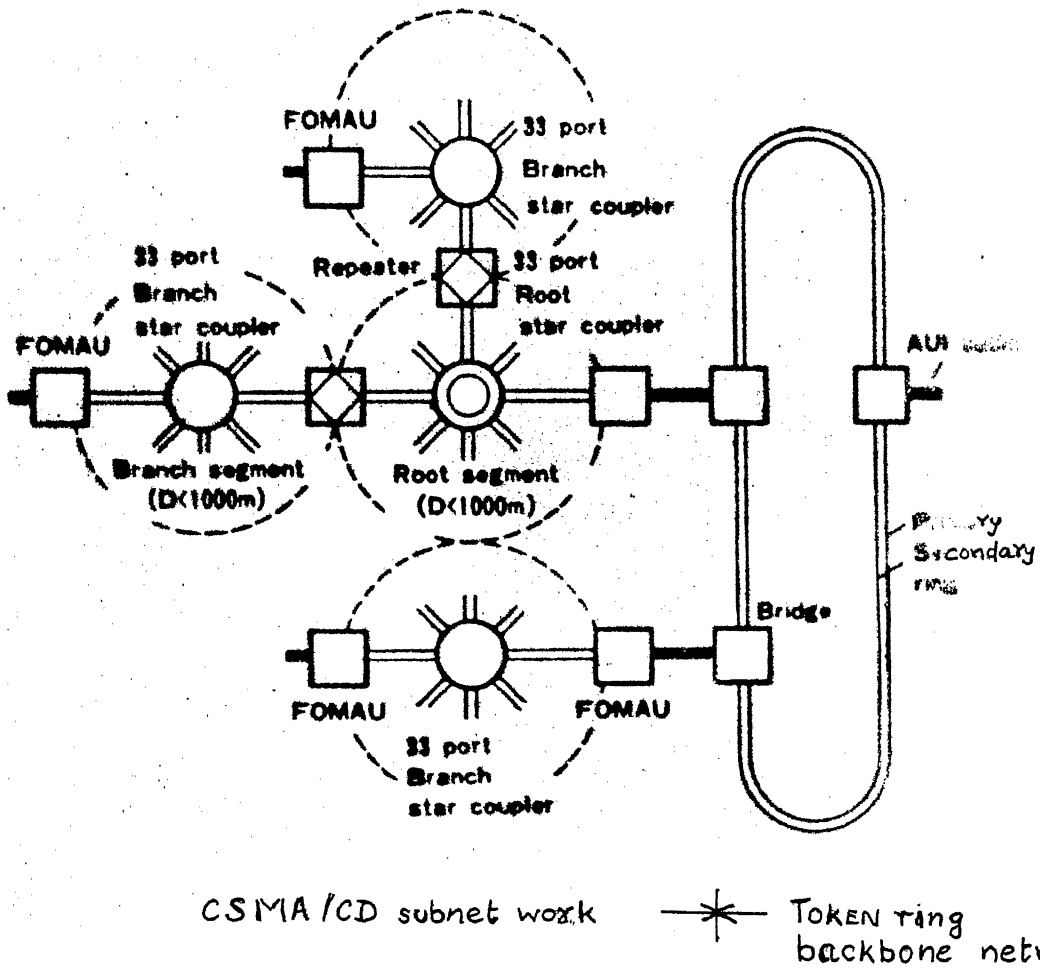


FIG. 2.1 CONFIGURATION OF A FIBER OPTIC PACKET LAN [16]

CSMA/CD subnetwork	Medium access method	CSMA/CD
	Information bit rate	10 Mbps
	Max. distance between FOMAU's	1 km. (without repeater) 3 km. (with repeater)
	Max. number of FOMAU's	32 (without repeater) 1024 (with repeater)
Token Ring Backbone Network	Medium access method	Token ring (FDDI based)
	Information bit rate	32 Mbps
	Max. distance between bridges	2 km. 4 km. (1 node bypassed)
	Max. number of bridges	64
	Max. total ring length	128

FOMAU : Fiber Optic Medium Attachment Unit

TABLE 2.1 : Main features of a fiber optic packet LAN

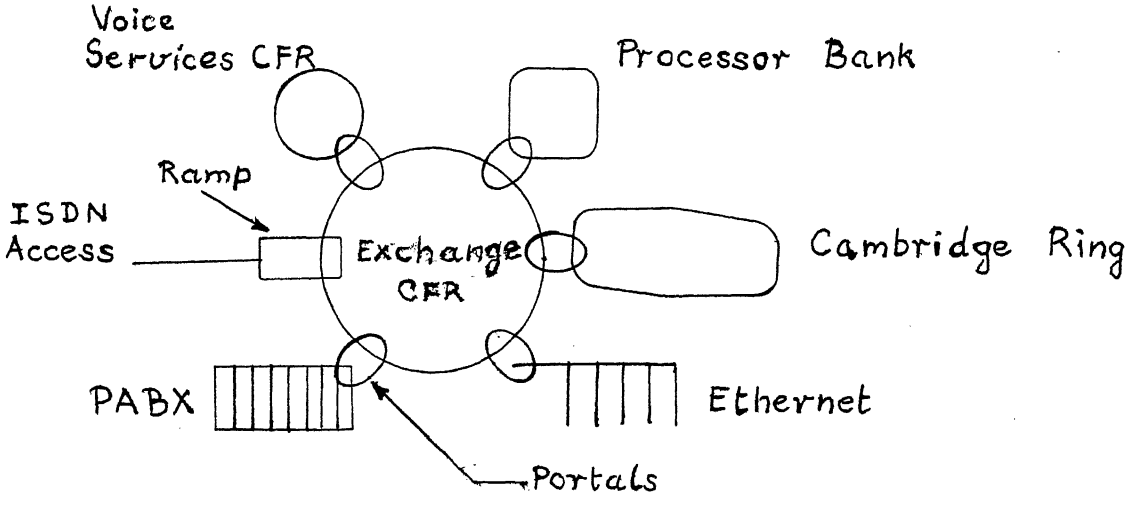


FIG.2.2 THE UNISON EXCHANGE [17]

2.3 ProNET-80 :[18,19]

ProNET-80 (Fig.2.3) is an 80 Mbps network configured as a star shaped ring. The network has a wire center at the hub of a star configured network. The wire center is passive and provides a way for users to break into the ring. Attachment to the ring is accomplished through a relay which is energized when the user desires to join the ring and is deenergised if the cable between the host and the wire concentrator snaps or if the host fails, thus by-passing the host. The relays are connected by counter rotating rings to increase the reliability of the network. The rings can support upto 255 users.

ProNET uses a token passing scheme for media access. It allows multiple packets per token. Further it permits variable number of data bytes in a packet because special control characters are used to indicate data field boundary. The maximum length of the data field is limited by the buffer size to 2044 bytes.

ProNET uses a 4B/6B coding scheme for line coding of data where every four bit pattern is assigned a six bit binary value. Of the 20 balanced six bit patterns available, 16 are selected to correspond to the 16 possible four bit patterns thus achieving a balance of one's and zero's in every string of six units. This scheme has a strong error checking mechanism built in, as the reception of a synchronized six bit word that is unbalanced indicates an error.

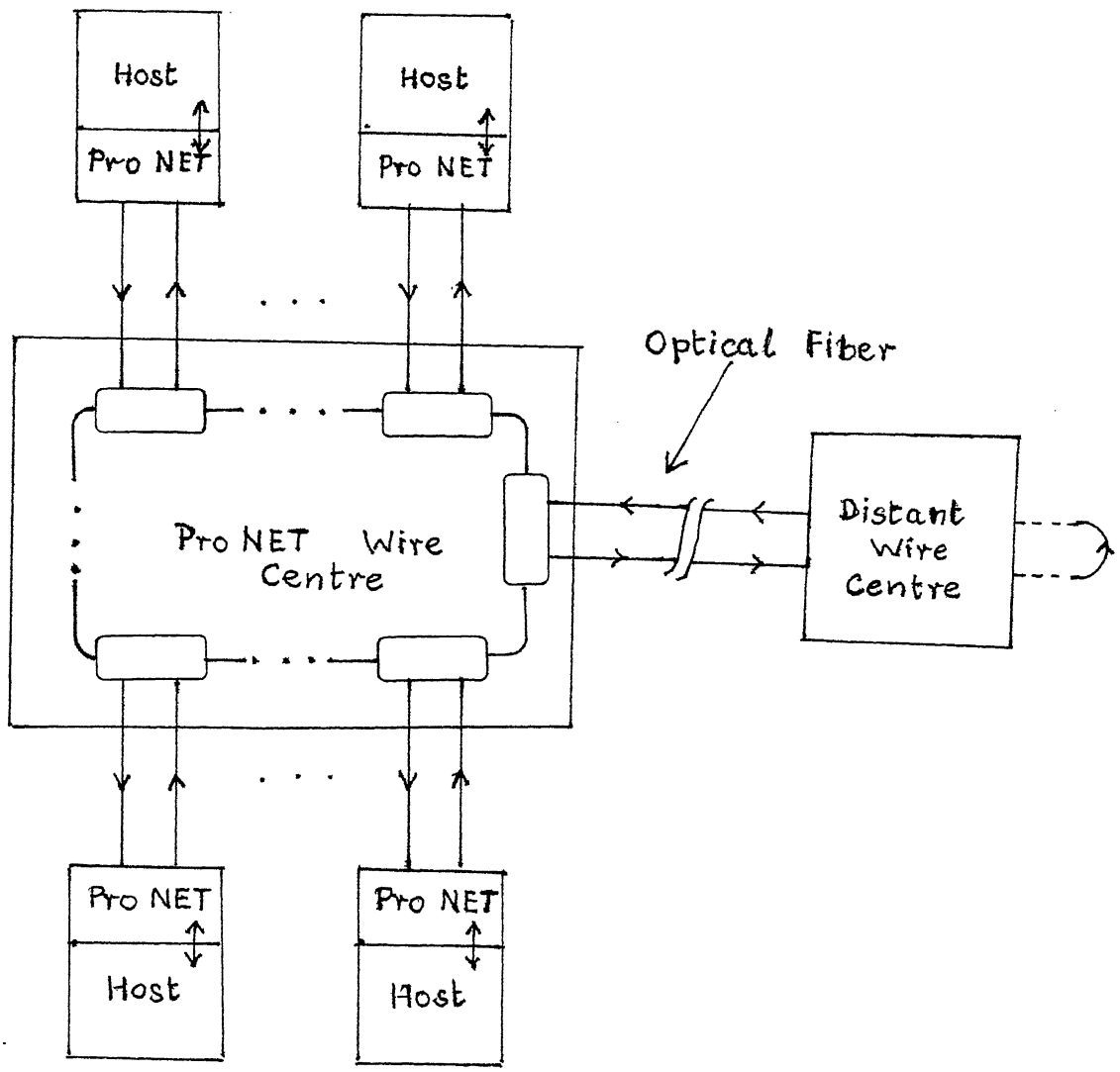


FIG. 2.3. CONFIGURATION OF Pro NET [18]

ProNET has been widely used as a backbone network to interconnect LANs such as Ethernet, Arpanet, the IBM token ring and ProNET-10.

2.4 FIBER DISTRIBUTED DATA INTERFACE [FDDI] :[4,20,21,22]

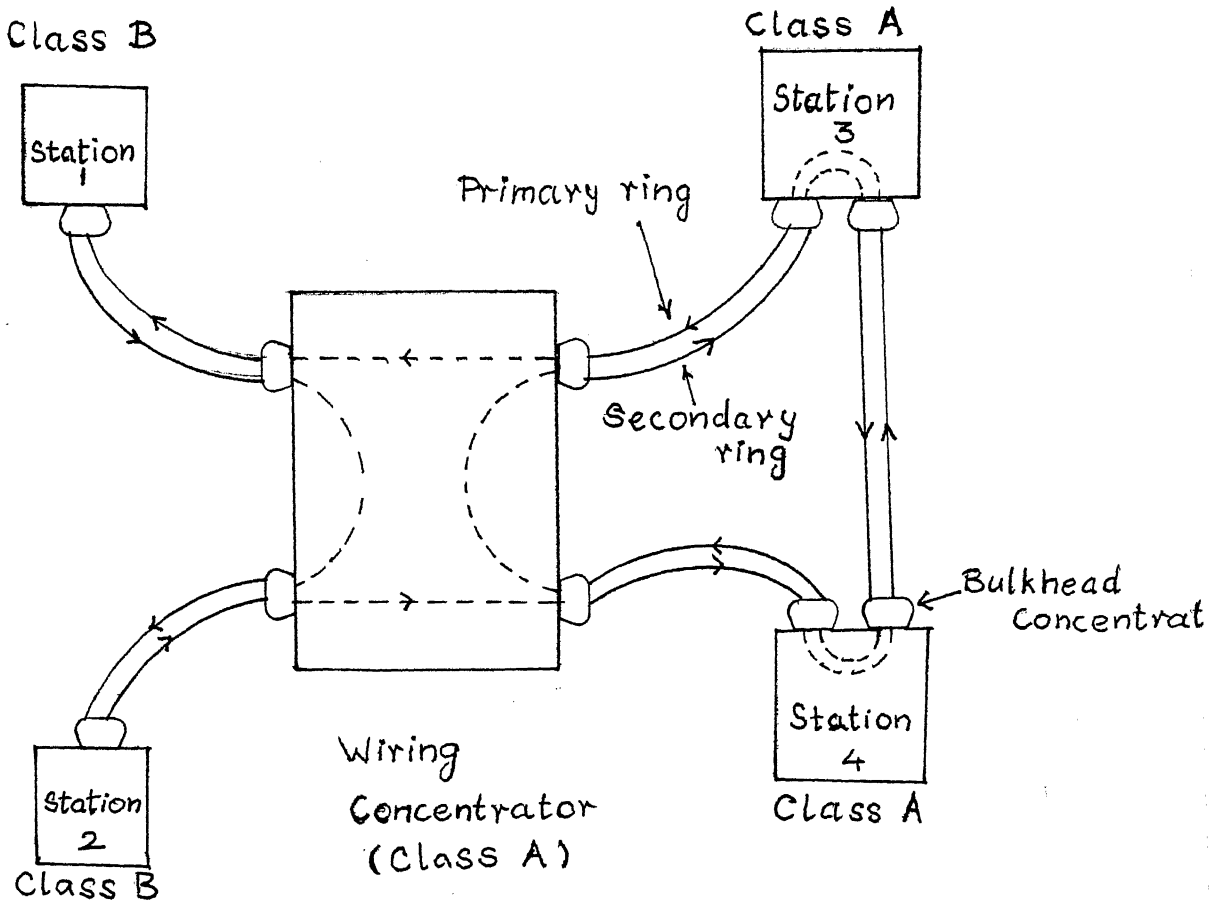
The FDDI is an American National Standards Institute [ANSI] specification for fiber optic local area networks. Some salient features of FDDI are discussed here.

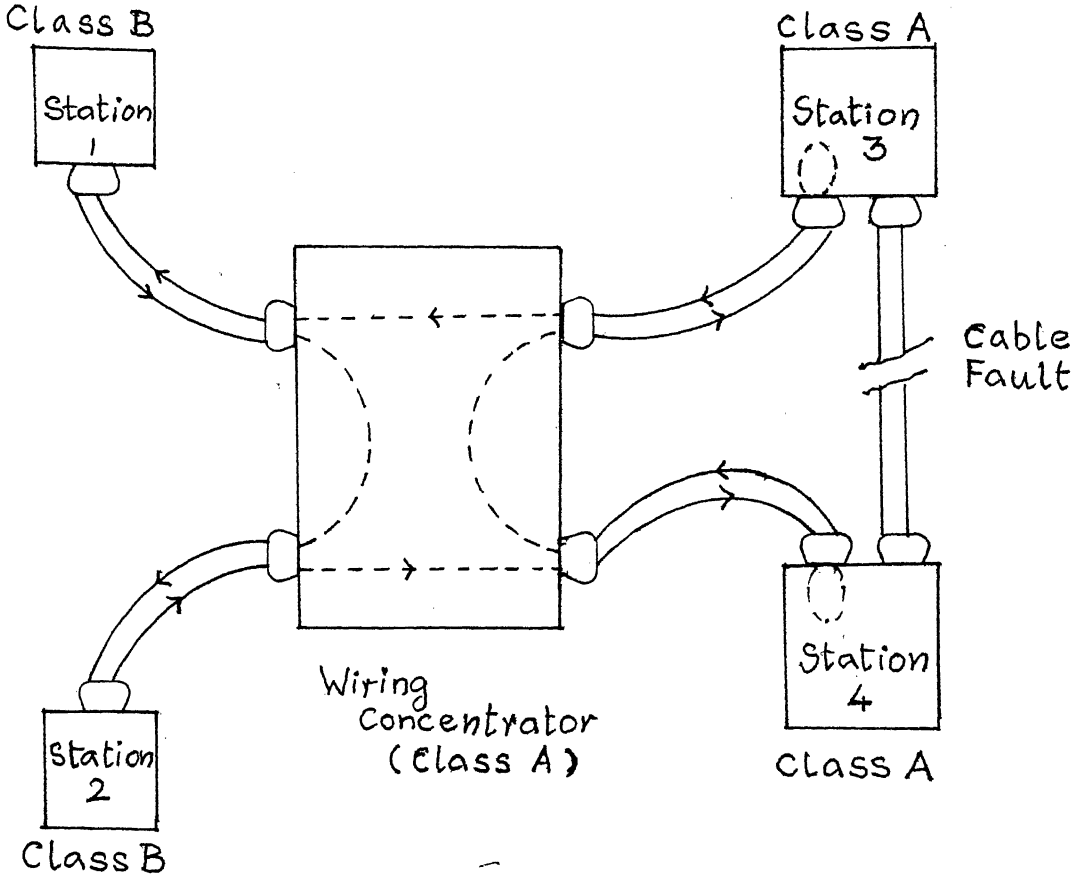
FDDI specifies a fiber optic ring which can support up to a maximum of thousand nodes and operates at 100 Mbps. The nodes can be as far as two km. apart and the ring circumference can be up to 200 km.. These limits are to minimize latency on the ring. ANSI has recommended a 4B/5B line code for FDDI.

FDDI specifies a topology in which two independent counter rotating rings are in place, which provide for an overall bit rate of 200 Mbps., with each ring operating at 100 Mbps. The components are tied together by a wiring concentrator as in Fig.2.4. The inner ring connects only certain systems which are critical. These systems are called class A devices and have both rings attached to them. The lower priority systems, called class B devices are connected only to the outer ring.

The wiring allows a facility to connect stations and provides for reconfiguration. Fig.2.5 provides a possible reconfiguration in the event of a lost channel or channels.

FIG. 2.4 FIBER DISTRIBUTED DATA INTERFACE [FDDI][





The FDDI access is based on a token packet which represents a permission to transmit. The token is called a timed token because there is a provision for specifying the time it takes a token to make a cycle of the ring called the token rotation time. As a part of the ring initialization process, the stations negotiate for a target token rotation time (TTRT), a parameter which specifies the expected token rotation time. Each station requests a value that is fast enough to support its synchronous traffic needs. The shortest requested time is assigned to Topr.; a parameter which specifies the operational TTRT . Topr. is used to limit the token rotation time.

Each station has a token rotation timer (TRT), which controls the stations access to the network. Each stations TRT is initialized to Topr.; it expires after a Topr. time period, and then it is reset to Topr. and enabled again. Each station contains a parameter Late-Ct., which records the number of times its TRT has expired since the token was last received at the station. Late-Ct. is initialized to zero. Whenever a station's TRT expires, its Late-Ct. is incremented. It is cleared each time the station receives the token. The token is considered to arrive at a station on time if its TRT has not expired since the station last received the token, i.e., if Late-Ct. is equal to zero. Otherwise, the token is considered to be late. If the token arrives at a station on time, its TRT is reinitialized to Topr.; otherwise its TRT continues to count towards expiration. Expiration of a station's TRT when Late-Ct. is equal to zero triggers

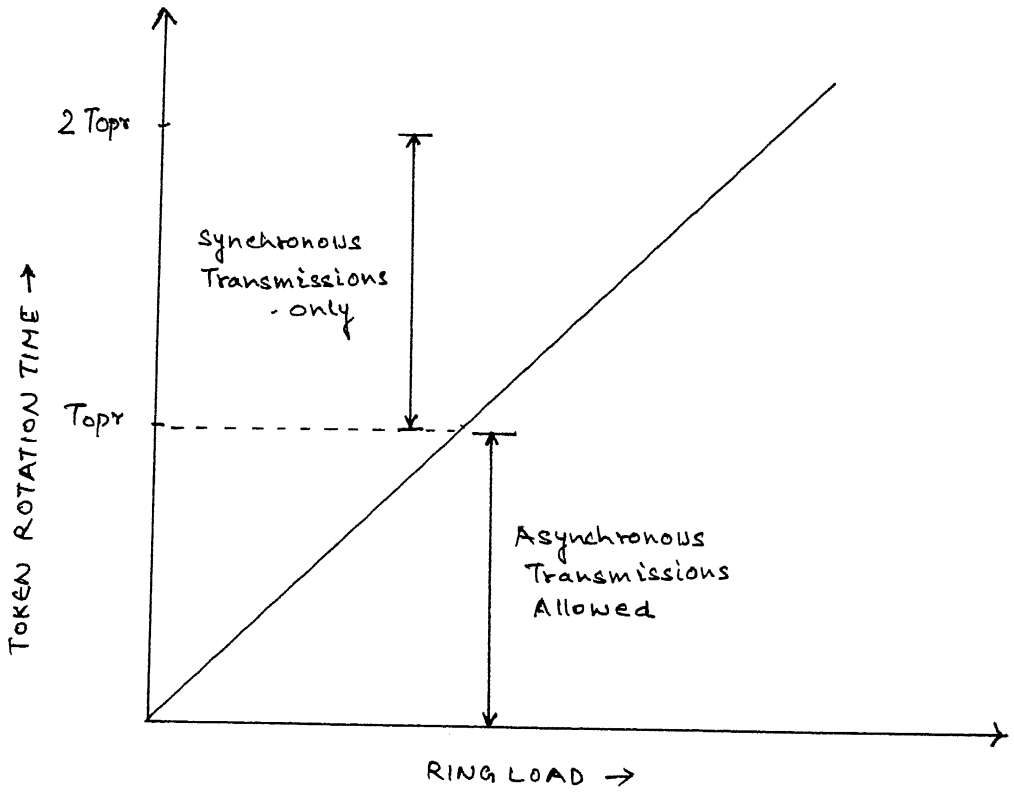


FIG. 2.6 : SYNCHRONOUS AND ASYNCHRONOUS TRANSMISSIONS IN FDDI - [5]

initialization of the ring recovery process. Hence during the negotiation for TTRT, (and thus for Topr.) each station should request a value that is half the token rotation time it requires to support its synchronous needs.

Each station is assigned a percentage of Topr. for its synchronous transmission. The total of all synchronous assignments should not exceed 100% of Topr.. Whereas a station may transmit synchronous frames for its allotted time whenever it receives a token, under normal operation it may initiate transmission of asynchronous frame only to the extent that the immediate preceding cycle of the token was less that Topr., which would be the case when the load on the ring is light. All bandwidth that is not used for synchronous transmission is available for a synchronous transmission. This is shown in Fig.2.6 assuming that the TRT is linearly related to the load on the ring.

2.5 CONCLUSION

In this chapter a review of backbone networks which supports voice and data traffic and a few important fiber optic ring networks has been carried out.

CHAPTER 3

SYSTEM DESIGN

In this chapter the design of a high speed digital network which can support voice and data traffic is carried out. The topology, the media access scheme used, frame and slot formats, line coding and the block schematic of the node are discussed.

The aim of this work is to design a high speed communication network which;

- can support voice and data traffic.
- has very high data rates.
- provides high throughput and minimum delay.
- is capable of transferring bulk data.
- provides 2.048 Mbps primary access ISDN path.

3.1 NETWORK TOPOLOGY

A slotted ring topology similar to the one used by Kamesh [4] is used. The principal difference is that while Kamesh has designed a network to support 64 Kbps PCM channels the present network is designed to support 2.048 Mbps channels which can provide primary access ISDN path.

The block diagram of the ring is shown in Fig.3.1. The nodes are connected by a single unidirectional cable. One of the nodes on the ring will do the ring monitoring functions as well as provide the timing information to the other nodes on the ring. This one is designated as the ring controller.

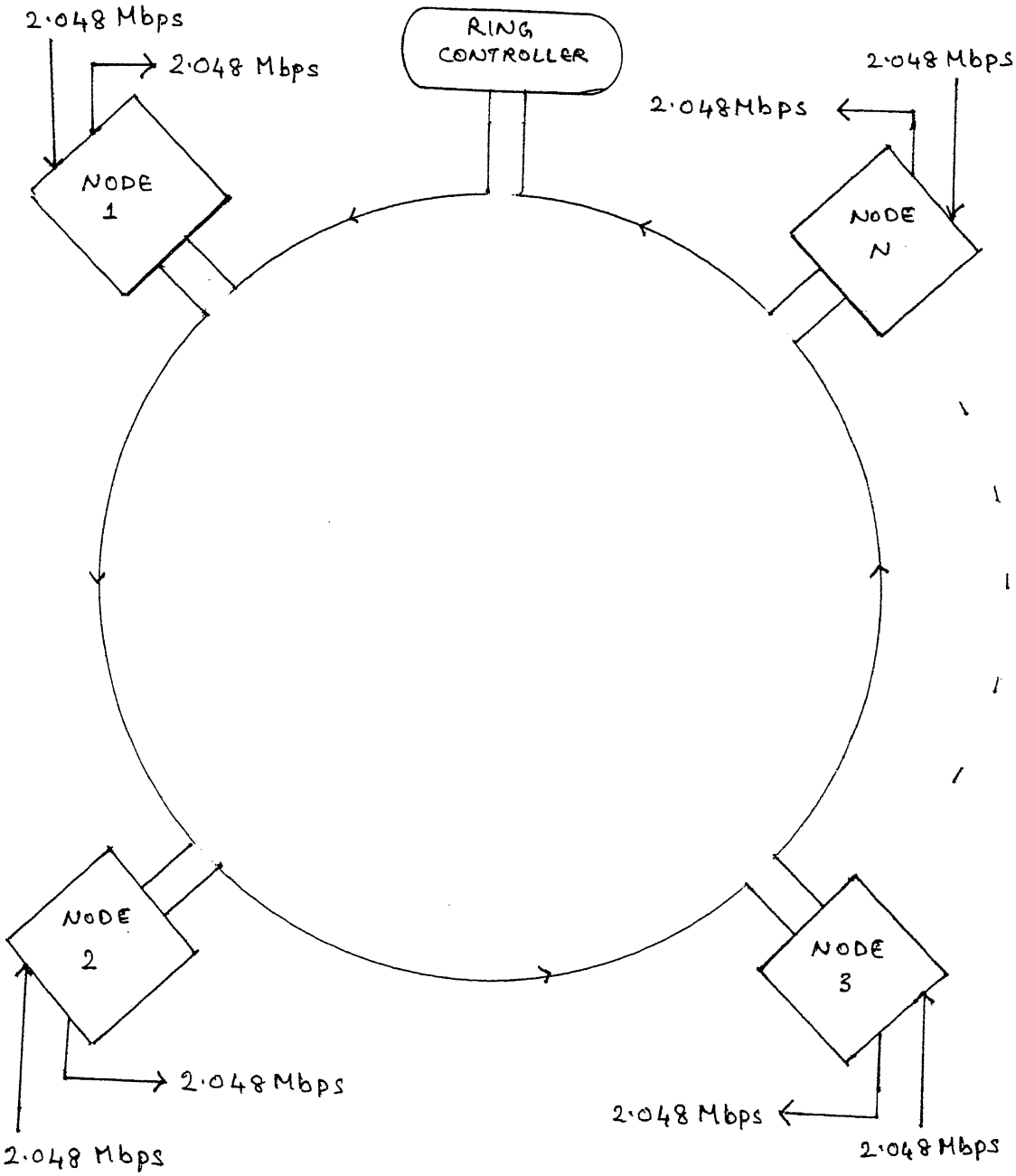


FIG. 31 : BLOCK SCHEMATIC OF THE NETWORK

The functions of the ring controller are mentioned in section 3.5.

It was pointed out in section 1.1 that a circuit switched approach is best suited for voice. A TDMA scheme with n slots per frame format meets this requirement and can support data as well. This structure is adopted.

3.1.1 Choice Of Frame Repetition Rate And Slot Size

Providing digital subscriber access based on a 64 Kbps channel is important for a network which has to cater to voice traffic. So each node on the ring accumulates one frame of data every 125 u sec. Thus the frame duration on the ring should be 125 u second or its multiples to keep the buffering minimal. This leads to a rate of 8000 frames per second.

Since each node is provided with access to a 2.048 Mbps channel, the node collects 256 bits of data every 125 u sec. Thus each slot should carry information corresponding to 256 bits of data.

3.2 LINE CODING

The raw binary data generated from a source is generally not suitable for transmission on a fiber optic channel due to the following reasons.

(1) Occasional disappearance of the timing information.

(2) Base line wander due to d.c. content in the data.

Line coding of the data is done before transmission to

overcome these problems and in addition to provide some error monitoring.

Two level Alternate Mark Inversion (AMI) codes and mB/nB block codes are the popular line codes used for high data rate communication systems.[23]. Of the mB/nB codes, the 1B/2B code also known as the Manchester code is very popular. Manchester codes and two level AMI codes need a bandwidth that is twice the baseband data rate and so these codes are not generally used for systems that have a baseband data rate greater than 10 Mbps.

For the present work a 4B/6B code has been chosen for the following reasons.

(1) It provides enough transitions to allow easy clock recovery. In the coding scheme chosen a minimum of three transitions are guaranteed within every code.

(2) It has an energy spectrum with a small low frequency component thereby minimizing d.c. wander.

(3) Provides error monitoring capability.

(4) It does not impose any restrictions on the input message sequence.

(5) Each code vector maps on to a unique data word and vice-versa independent of the status of the encoder/decoder.

(6) Since data is coded in blocks of four bits, the scheme matches well with the available fast RAMs that have been used for time division switching.

(7) There are enough unused code words which could be made

use of for control signaling and synchronization purposes.

(8) The code obviates the need for bit stuffing/destuffing.

(9) The hardware required to implement the encoder and the decoder are simple.

The 4B/6B coding scheme used is given in Table 3.1.

3.3 FRAME AND DATA SLOT FORMATS

The frame format is shown in Fig.3.2(a). The frame is divided into 8 equal slots, each carrying information corresponding to 256 bits of data (384 bits after encoding). The first seven slots of the frame are data slots while the last slot is dedicated to signaling and is used to implement the media access protocol. The contents of the signaling slot are discussed in section 3.4.1.

The format of a data slot is shown in Fig.3.2(b). The data slots are delimited using a unique 6 bit word called the Slot Synchronization Word (SSW) which is a 6 bit pattern 000111. The end of the frame is indicated by another unique word called the Frame Synchronization Word (FSW) which is the 6 bit pattern 111000. These two synchronization words are unique patterns in that these patterns are not used as code words for any data sequence and in addition even a concatenation of two code words cannot produce such a pattern in the coded bit stream. (Refer Table 3.1).

3.4 MEDIA ACCESS PROTOCOL

It was mentioned in section.3.1 that the network uses

Sr. No.	4B Word	6B Word			
		Positive Group	Following Group	Negative Group	Following Group
1	0000	110010	+	110010	-
2	0001	100110	+	100110	-
3	0010	110101	-	100100	+
4	0011	110100	+	110100	-
5	0100	010110	+	010110	-
6	0101	010101	+	010101	-
7	0110	010011	+	010011	-
8	0111	011010	+	011010	-
9	1000	100101	+	100101	-
10	1001	101001	+	101001	-
11	1010	101010	+	101010	-
12	1011	001011	+	001011	-
13	1100	011001	+	011001	-
14	1101	011011	-	001010	+
15	1110	101100	+	101100	-
16	1111	001101	+	001101	-

TABLE 3.1 : 4B/6B CODING SCHEME

TDMA scheme. In addition to providing virtual circuit switched path, TDMA has the following advantages.

(1) Provides high throughput under heavy load conditions .

(2) Fixed delay once the connection is established.

3.4.1 The Signaling Slot

The signaling slot is used to implement the protocol. The bit assignment of the signaling slot is given in Fig.3.3. There are seven reservation bits (marked A to G) within the first 18 bits (3 six word patterns) . A node can set any one of these bits to reserve a slot. Setting bit A reserves the first slot, bit B the second slot and so on. It is reasonable to assume that a node in want of a slot will reserve the earliest slot it finds free. The node which has reserved a slot, has the slot for the as long as it wants and resets the reservation bits at the end of its transmission thus relinquishing the slot. Of these 18 bits all bits other that the reservation bits and permanently set or reset as shown Fig.3.3. This pattern has been chosen to ensure that the SSW or FSW does not occur within the signaling slot.

The addressing of the slots is done using the next 28 six bit words (bit 19 to 188). Each node is assigned an 8 bit address. The address is also encoded 4B/6B and so consumes 12 bits. (Two six bit words). If a node has reserved the first slot it loads the address of the destination slot followed by its own address in the space earmarked for addressing the first slot. The destination

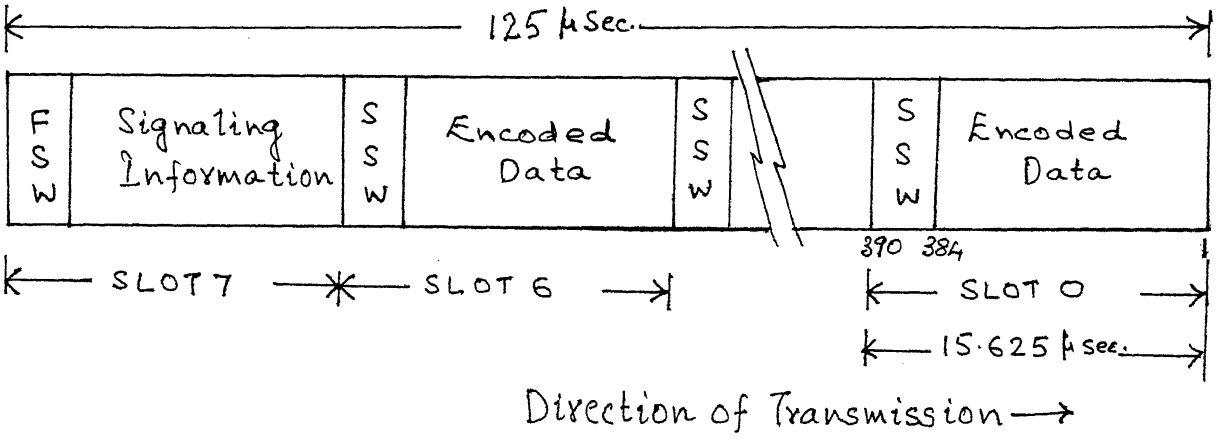


FIG. 3.2 (a) FRAME FORMAT

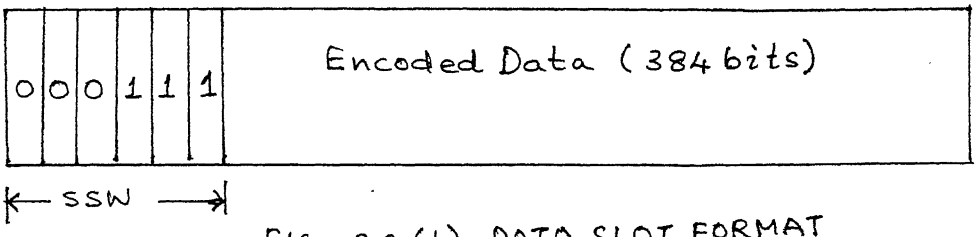


FIG. 3.2 (b) DATA SLOT FORMAT

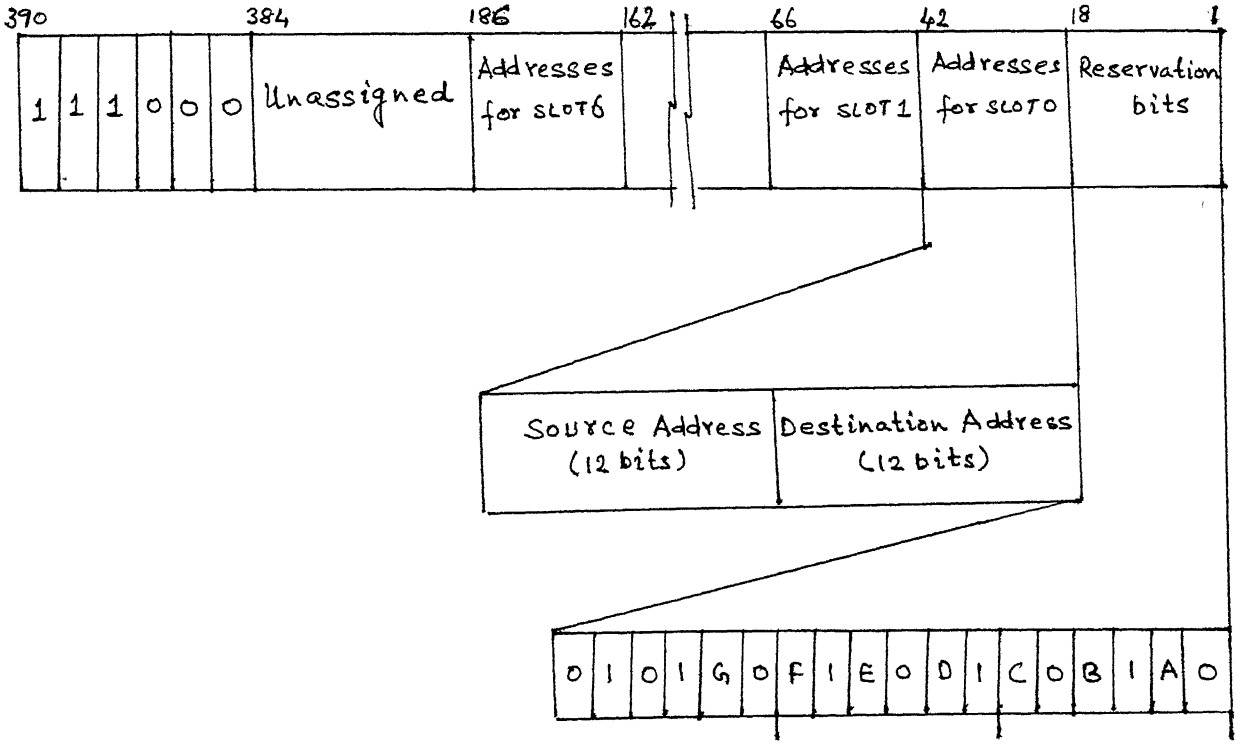


FIG. 3.3 SIGNALING SLOT FORMAT

acknowledges the call by reversing the order of addresses. Non reversal of the addresss is treated as a negative acknowledgment. If a node receives the acknowledgment for its request for transmission it grabs the reserved slot, fills it with 384 bits of data (encoded version of 256 bits.) and follows it up with the SSW. The destination node does not acknowledge any other call until the current call is cleared. The destination node decodes the data in the slot meant for it and stores it in a RAM from which the external source reads it during the next frame.

3.5 RING CONTROLLER

The presence of a ring controller was mentioned in section 3.1. The last slot (8th) on the ring is assigned to the ring controller. The first 188 bits of this slot are used for reservation and addressing. The ring controller is expected to perform the following functions;

(1) Act as a master clock source for the entire system

(2) Provide framing information by sending FSW.

(3) Provide enough buffering to allow integral number of frames on the ring.

(4) Monitor the proceedings in the ring by looking into reservation bits and addresses.

(5) Provide toll information

3.6 DATA RATE CALCULATIONS

Each node communicates with the host at a rate of 2.048 Mbps. So in every 125 u sec., the node collects 256 bits.

Since the data is encoded 4B/6B before transmission the total number of encoded bits is 256x6/4 = 384 bits. These 384 bits are to be transmitted in a time slot of duration 125/8=15.625 u sec. In addition the six bit synchronization word should also be transmitted in the slot itself. Thus the data rate on the ring is 390/15.625 = 25.344 Mbps.

3.7 THE NODE

The block schematic of the node is given in Fig.3.4. The node is expected to perform the following functions.

(1) Receive the serial data stream and retransmit it. If the data is meant for the node then it has to be tapped and transmitted to the host.

(2) Transmit the data collected during the last 125 u sec. on the ring during the reserved time slot and follow it up with the SSW.

(3) Assist the user in setting up and relinquishing a call.

(4) Recover the clock and maintain bit synchronization.

(5) Recognize the SSW and FSW and use this information to update the status information of the ring and to establish word synchronization.

(6) By pass the node in case of a fault.

3.7.1 Functional Description of the Node

The encoded data from the receiver is fed to the input of the front end processor. The processor recovers the clock, identifies the six bit coded words and assigns/deassigns slots based on the requests from the host.

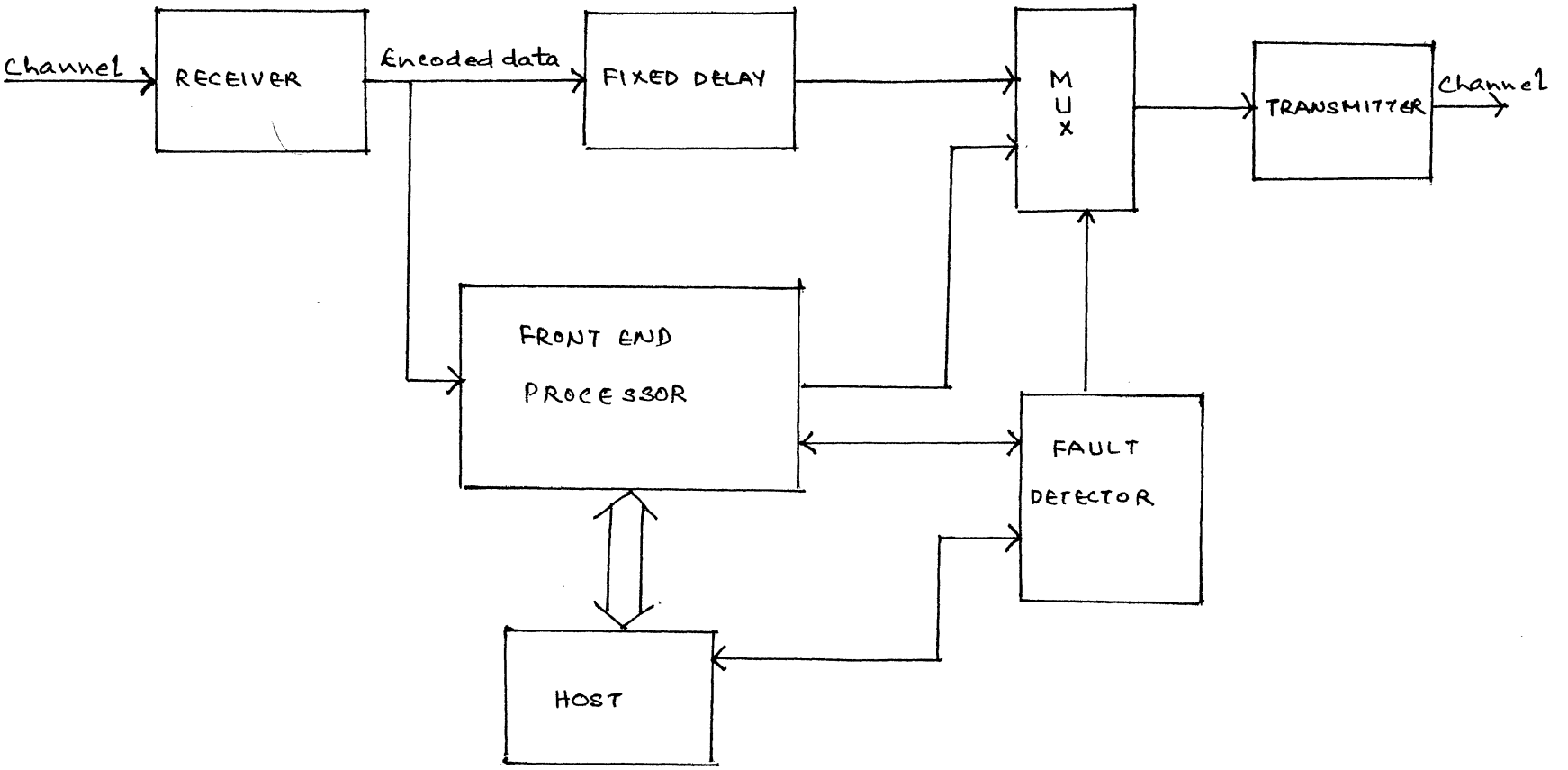


FIG. 3.4 : BLOCK SCHEMATIC OF THE NODE

It encodes the data from the host and transmits it on the ring. Data meant for the host is decoded and handed over to the host. The fault detection circuit bypasses the node and blindly transmits the input data stream after fixed delay in case of a node failure.

3.8 CONCLUSION

In this chapter the design of a high speed TDM ring network which supports eight slots per frame and is suitable for voice and data traffic has been carried out. The synchronization technique and the line coding scheme used have been discussed in detail. The block schematic of the system and of the individual node has been arrived at.

CHAPTER 4

HARDWARE IMPLEMENTATION

The details of implementation of the node front end processor which comprises of the clock recovery and synchronization circuits, encoder, decoder and the signaling processor are discussed in this chapter.

4.1 CLOCK RECOVERY AND SYNCHRONIZATION CIRCUITS

The block diagram of the clock recovery and synchronization circuit is given in Fig.4.1. The input to the module is the encoded data. The outputs of the module are;

(1) The recovered clock, Fd.

(2) The word synchronization signal, WS.

(3) The synchronized encoded data word, D0-D5.

(4) The slot synchronization signal (SS) which goes high when SSW is detected.

(5) The frame synchronization signal (FS) which goes high when FSW is detected.

(6) The signal AS which is high when SS or FS is high.

(7) The frame counter output FC (one bit) which indicates if the received frame is an odd or even frame.

(8) The slot counter output (3 bits) which indicates the number of the slot which is currently being received.

(9) The signal SY which is an indication to the encoder (if it is transmitting data) that it has completed transmitting the allotted 32 bytes of data and now has to follow it up with the SSW and relinquish the

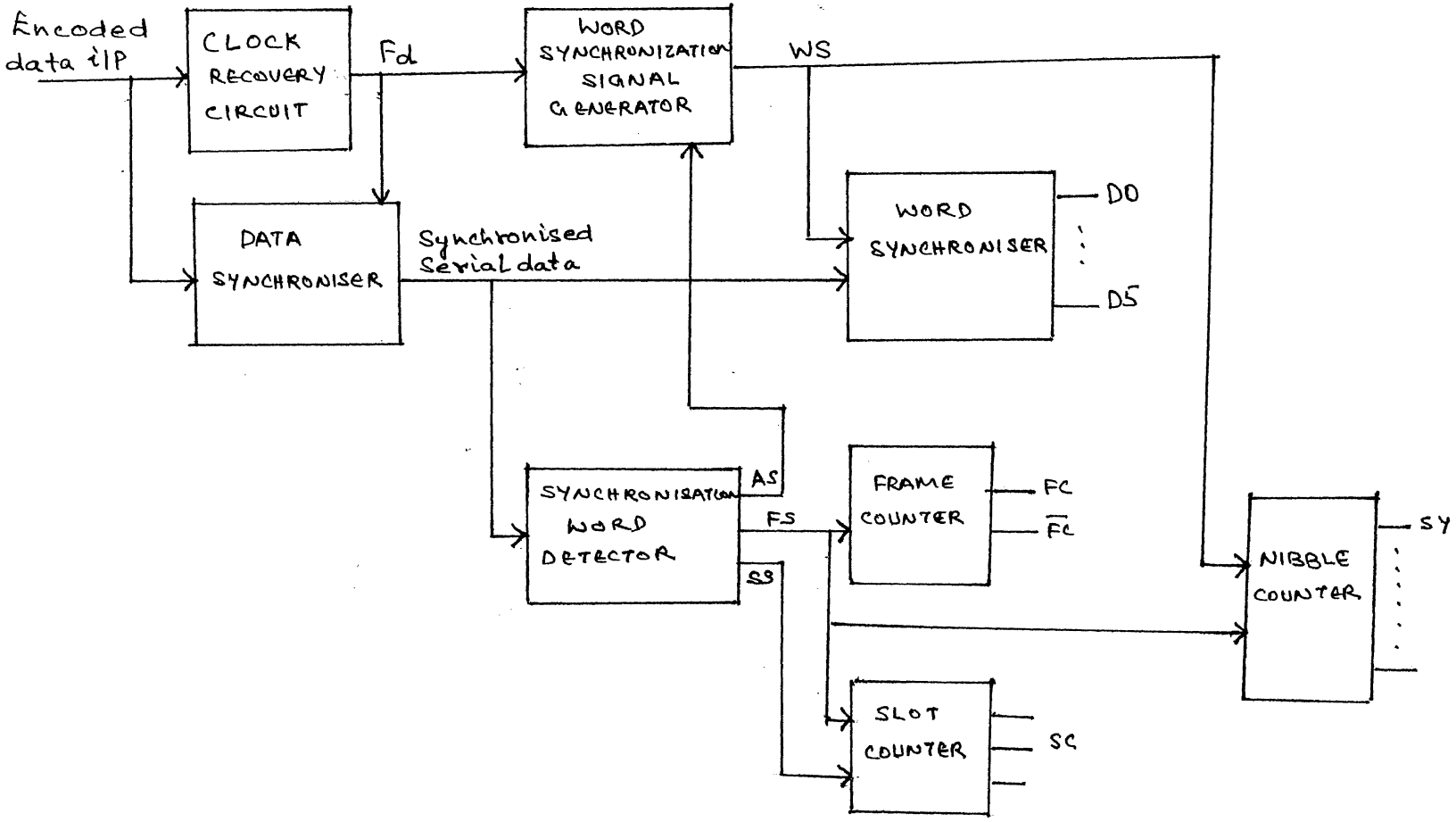


FIG. 4.1. : BLOCK SCHEMATIC OF CLOCK RECOVERY AND SYNCHRONIZATION CIRCUITS

channel.

4.1.1 Clock Recovery

It was mentioned in Sec.3.2. that the transmitted data is encoded 4B/6B. The code words have enough transitions which make the clock recovery easy. Clock is recovered from the encoded data using the delay-EXOR technique. (Fig.4.2).[24]. A positive spike is obtained at the EXOR output for every edge in the input sequence. The spectrum of the waveform at the EXOR gate output consists of a continuous spectrum with discrete spectral lines at multiples of the symbol rate frequency. A narrow band pass filter can be used to pass the discrete line at the symbol rate frequency and to suppress adjacent continuous spectral components. The PLL can be considered to be a narrow band tracking filter which reconstructs a stable timing reference whose period is locked to the estimated average of the interval between the rising (or falling) edges of the EXOR output. The PLL will lock on to the desired spectral line only when a sufficient number of transitions are seen by the phase detector. This is ensured by the line coding scheme.

The circuit diagram of the clock recovery circuit is given in Fig. 4.3. The data is fed to one input of an EXOR gate (IC18/1) and the delayed data (delayed by four NOT gates, IC15/1 through IC15/12) is fed to the other input (IC18/2). The detected edges are capacitively coupled to one input of the PLL, XR-215 (IC21/4). The other input to the PLL (IC21/6) is the clock output of a comparator (IC26/11). One

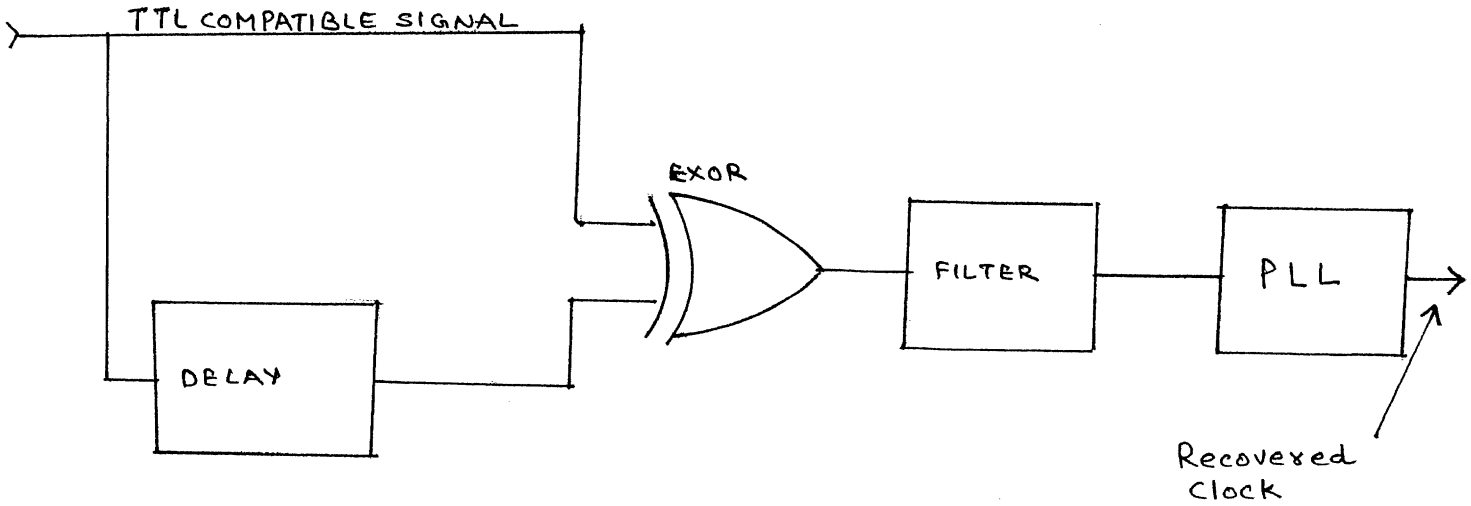


FIG. 4.2 : CLOCK RECOVERY USING DIGITAL GATES AND PLL [24]

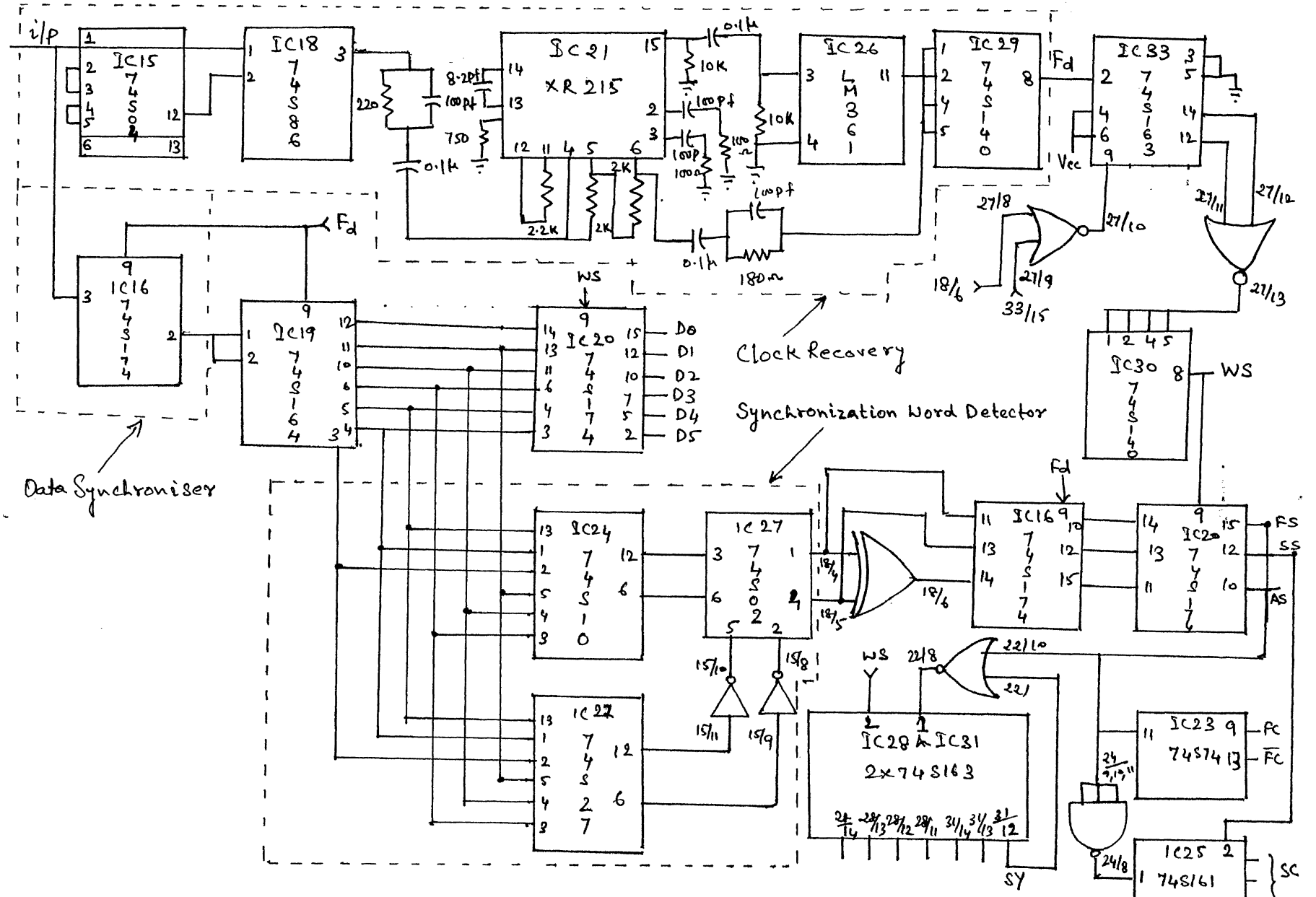


FIG. 4·3 : CIRCUIT DIAGRAM OF CLOCK RECOVERY AND SYNCHRONIZATION CIRCUIT

input of this comparator (IC26/8) is the VCO output of the PLL (IC21/15) and its other input is grounded. The biasing components for the PLL and the value of the timing capacitor for the VCO was chosen as per the guidelines in the application note.[25]. The clock output is passed through a driver (IC29) and its output (IC29/8) Fd is made available to the other circuits on the node.

4.1.2 Data Synchronizer The input data is fed to a D F/F (IC16/3) which is clocked by Fd. The synchronized data is available at the output of the D F/F (IC16/2).

4.1.3 Synchronization Word Detector

The synchronized data is fed to the input of a serial to parallel converter (S/P) (IC19/1). The block labeled Synchronization Word Detector in Fig.4.3 detects the SSW and FSW. The output of one NOR gate (IC27/1) is high on detecting a FSW and that of the other (IC27/4) is high on detecting a SSW. The output of the EXOR gate (IC18/6) is high on detecting either SSW or FSW. The outputs of the NOR gates and the EXOR gate are fed to the D F/F inputs (IC16/11,13,14) which is clocked by Fd to introduce a delay. The outputs of the D F/Fs (IC16/10,12,15) are fed to another D F/F (IC20/14,13,11). The D F/F outputs (IC20/15,12,10) are the Frame Synch. (FS), Slot Synch. (SS) and AS signals. FS and AS are high for six clock pulses if a FSW is detected. SS and AS are high if a SSW is detected. The D F/Fs last mentioned are clocked by the Word Synchronization signal WS which is generated as follows.

4.1.4 Word Synchronizer

Since the FS, SS and the AS signals are to be held for six bits duration the latching signal is the output of a counter which divides Fd by six. So Fd is fed to a counter (IC33) connected in the divide by six mode. The parallel enable of the counter (IC33/9) is an ORed version of the divide by six output (IC33/15) and the EXOR output (IC18/6). The parallely loaded output of the counter is detected by a NOR gate and its output, (IC27/13) WS is fed to a driver (IC30/1). The driver output (IC30/8) goes high one Fd pulse after AS goes high. Thus WS acts as a word synchronizer. This WS is also used to latch the 2nd to 7th bit of the S/P on to a D latch. The output of the D latch (IC20/15,12,10,7,5,2) gives the synchronized word D0 to D5.

4.1.5 Frame, Slot and Nibble Counters

The FS signal is fed as a clock to a D F/F connected in the toggle mode and so the output of the D F/F (FC) (IC23/9) indicates if the current frame is an even frame or odd frame.

The SS signal is fed as the clock to a 4 bit counter connected in the divide by eight mode. The output of the counter (IC25/14,13,12,11) gives the slot count.(SC). The counter is cleared asynchronously by the FS signal.

The WS signal is fed as a clock to a divide by 65 counter which is constructed by cascading two 4 bit counters. (IC28 and IC31). The counter is cleared by the ORed

version of AS and divide by 65 output (IC28/1) so that the counter is cleared immediately after the appearance of a synchronization word and from then on counts the six bit patterns each of which contains one nibble of data in its encoded form. When the FS is obtained, the nibble counter reads 64 indicating that it is the last nibble.

4.2 THE ENCODER

The input to the encoder module is the information of the allowed slot to transmit which it receives from the signaling processor. Apart from this, the clock recovery and synchronization module provides it with the synchronized and coded word (D0-D5), WS, FC, AS and Fd. The circuit diagram of the encoder is given in Fig.4.4.

When the node does not transmit the encoder converts the received coded word to serial (IC48) and transmits it. The parallel to serial (P/S) converter is loaded by the WS signal and the data shifted out by the recovered clock Fd.

The received coded word and the coded word of the data generated by the node are fed to tristate buffers (IC56 and IC40 respectively), the outputs of which are tied and fed to D F/Fs (IC49) clocked by the WS signal before the coded word is fed to P/S (IC48). Only one of the two buffers is enabled at a time based on the slot reserved by the node. This information obtained from the signaling processor is passed through a D F/F to whose outputs (IC45/5 and IC45/6) are used to enable one of the two buffers.

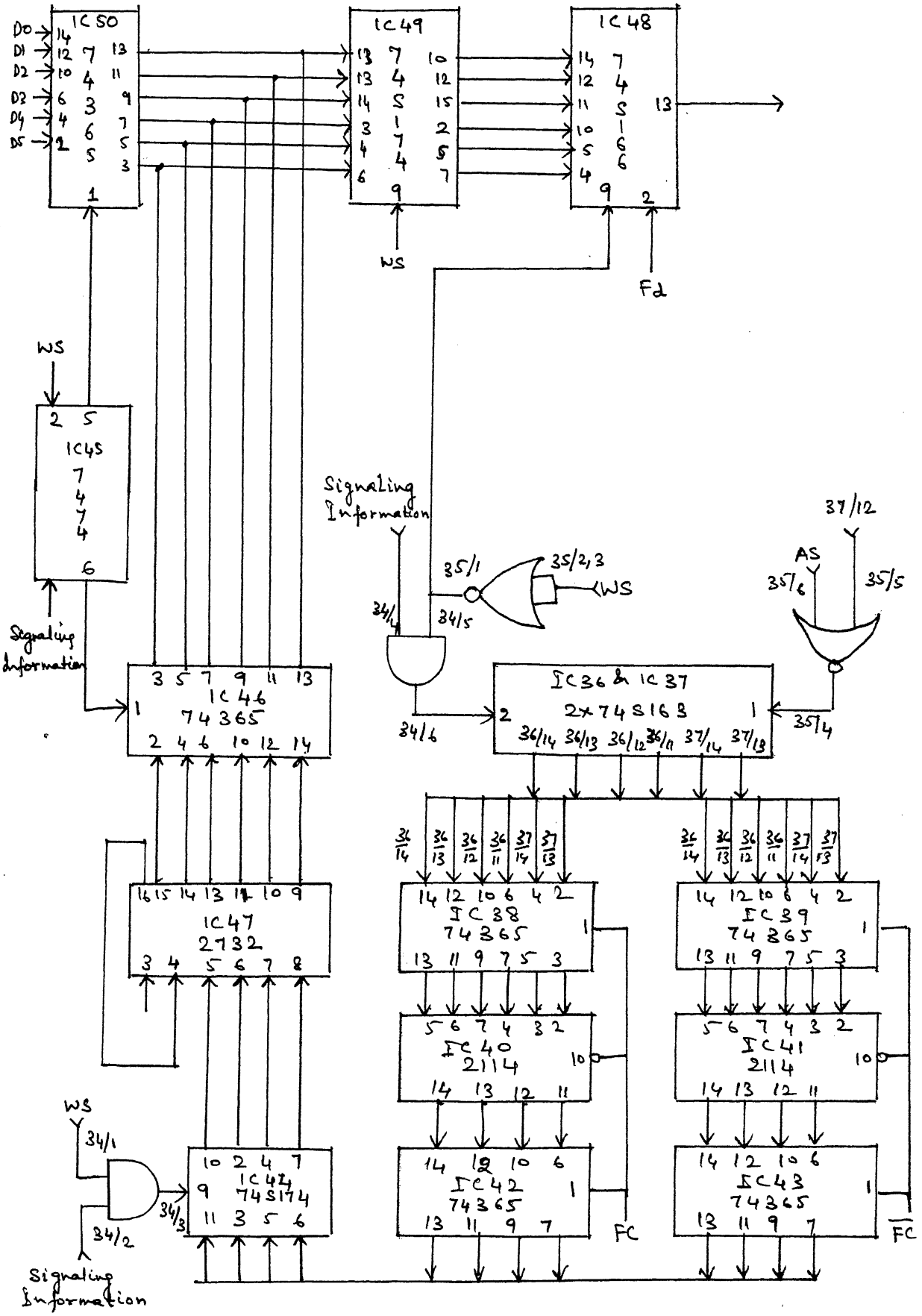


FIG. 4.4: CIRCUIT DIAGRAM OF THE ENCODER

If the present slot is not meant for the node, IC56 (tristate buffer) is enabled whereby the received data is transmitted after a fixed delay (called latency of the node) without any modification. The designed node has a latency of 40 bits.

If the present slot is meant for the node IC46 (tri state buffer) is enabled, the input of which is fed from the encoder EPROM (IC47).

The encoder has an address generator which is a divide by 65 counter obtained by cascading two four bit counters (IC36 and IC37). WS is the clock to the counter and is enabled if the present slot is the one allotted to the node, in which case a burst of 65 clocks are fed to the counter. The counter is cleared by the AS signal ORed with the divide by 65 output.

The encoder uses a 2RAM-2bank switching architecture. [25]. The address output of the address generator (IC36/14,13,12,11 and IC37/14,13) is fed to two tristate buffers. (IC38 and IC39). The output of each of these buffers are connected to the address inputs of identical high speed RAMs. (IC40 and IC41). The data output of each of the RAMs is buffered through a tristate latch. During the odd frame the address and data buffers of one of the RAMs are enabled (say IC38 and IC42) and that of the other (IC39 and IC43) are enabled during the even frame. If during a frame data is transmitted from one RAM, the data will be written into the other RAM from the external source during the same frame and

vice versa. When the buffers of a RAM are enabled the RAM is connected in the read mode. In the write frame, the RAM is connected in the write mode and data is written nibble by nibble into the address supplied by the external source.

The outputs of the data buffers (IC42 and IC43) are tied and connected to a D latch (IC44) to provide a delay before it is fed as the four LSB bits of the encoder EPROM address. (IC47/5,6,7,8). The fifth address bit of the EPROM is its seventh data bit which takes care of the group change over in the 4B/6B code. The sixth address bit is connected to the SY signal which indicates the 65th nibble corresponding to which the signaling word has to be sent. When this bit is high the EPROM outputs the signaling word. (SSW or FSW). The contents of the EPROM for an ordinary node are given in Table 4.1 and that for the node processor in Table 4.2. The timing diagram of the encoder is shown in Fig.4.5.

The switching could have been achieved using shift register as the buffer memory in which case the switching speed can be increased to approximately the shift register speed. [26]. However the amount of hardware required for such switches increase in the order of n , where n is the number of channels. [27]. When RAM is used as the buffer memory, the switching capacity is much larger than when shift registers are used,but the switching speed in such cases is determined by the access time of the RAM.

4.3 THE DECODER :

The input to the decoder module is the signaling word

Address A5-A0	Data D6-D0	Address A5-A0	Data D6-D0
000000	0000000	100000	0000111
000001	0100110	100001	0000111
000010	1100100	100010	0000111
000011	0110100	100011	0000111
000100	0010110	100100	0000111
000101	0010101	100101	0000111
000110	0010011	100110	0000111
000111	0011010	100111	0000111
001000	0100101	101000	0000111
001001	0101001	101001	0000111
001010	0101010	101010	0000111
001011	0001011	101011	0000111
001100	0011001	101100	0000111
001101	1001010	101101	0000111
001110	0101100	101110	0000111
001111	0001101	101111	0000111
010000	1110010	110000	1000111
010001	1100110	110001	1000111
010010	0110101	110010	1000111
010011	1110100	110011	1000111
010100	1010110	110100	1000111
010101	1010101	110101	1000111
010110	1010011	110110	1000111
010111	1011010	110111	1000111
011000	1100101	111000	1000111
011001	1101001	111001	1000111
011010	1101010	111010	1000111
011011	1001011	111011	1000111
011100	1011001	111100	1000111
011101	0011011	111101	1000111
011110	1101100	111110	1000111
011111	1001101	111111	1000111

TABLE 4.1 : Encoder EPROM Contents of Ordinary Node

Address A5-A0	Data D6-D0	Address A5-A0	Data D6-D0
000000	0000000	100000	0111000
000001	0100110	100001	0111000
000010	1100100	100010	0111000
000011	0110100	100011	0111000
000100	0010110	100100	0111000
000101	0010101	100101	0111000
000110	0010011	100110	0111000
000111	0011010	100111	0111000
001000	0100101	101000	0111000
001001	0101001	101001	0111000
001010	0101010	101010	0111000
001011	0001011	101011	0111000
001100	0011001	101100	0111000
001101	1001010	101101	0111000
001110	0101100	101110	0111000
001111	0001101	101111	0111000
010000	1110010	110000	1111000
010001	1100110	110001	1111000
010010	0110101	110010	1111000
010011	1110100	110011	1111000
010100	1010110	110100	1111000
010101	1010101	110101	1111000
010110	1010011	110110	1111000
010111	1011010	110111	1111000
011000	1100101	111000	1111000
011001	1101001	111001	1111000
011010	1101010	111010	1111000
011011	1001011	111011	1111000
011100	1011001	111100	1111000
011101	0011011	111101	1111000
011110	1101100	111110	1111000
011111	1001101	111111	1111000

TABLE 4.2 : Encoder EPROM Contents of Node Controller

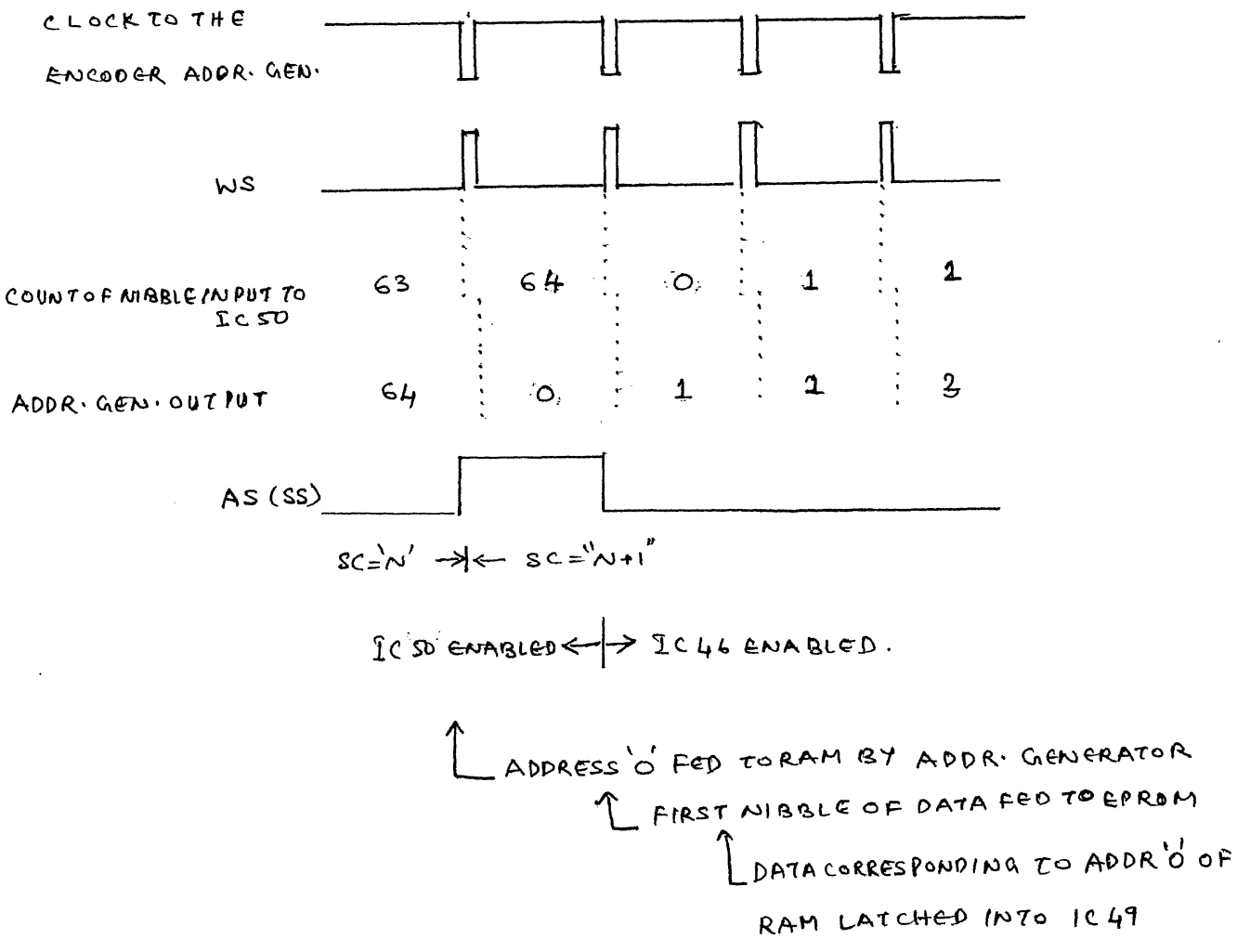


FIG.4.5 : TIMING DIAGRAM OF THE ENCODER

(one bit) from the signaling processor which informs the node at the beginning of a slot if the contents of that particular slot are meant for the node or not. Apart from that the clock recovery and synchronization module provides it with LE, FS and FC signals in addition to the synchronized encoded word. The circuit diagram of the decoder is given in Fig.4.6.

The decoder also uses a 2RAM-2bank architecture. Data is written into a RAM during a frame and is read out during the next frame. When data is being written into one of the RAMs it is being read out of the other RAM.

An address generator which is a divide by 65 counter is obtained by cascading two 4-bit counters (IC3 and IC4). It is clocked by the WS signal. The clock is enabled on obtaining the signaling word. Once enabled, it provides a burst of 65 pulses. Since only one slot in a frame can be addressed to the node, the counter is cleared by the FS signal ORed with the divide by 65 output.(IC4/12). The counter output (IC3/14,13,12,11 and IC4/14,13) is latched through a D F/F (IC5) clocked by the WS signal and fed through the tristate buffers (IC6 and IC7) to the two RAM chips (IC8 and IC9).

The synchronized word if meant for the node, is made available at the buffer output (IC14) by the signaling word and is fed to the decoder EPROM (IC13) which does the 4B/6B decoding. The contents of the EPROM is given in Table 4.2. The 4-bit output of the decoder is the data. This is latched through a D F/F (IC12) clocked by the WS signal and fed through buffers (IC10 and IC11) to the respective RAMs.(IC8

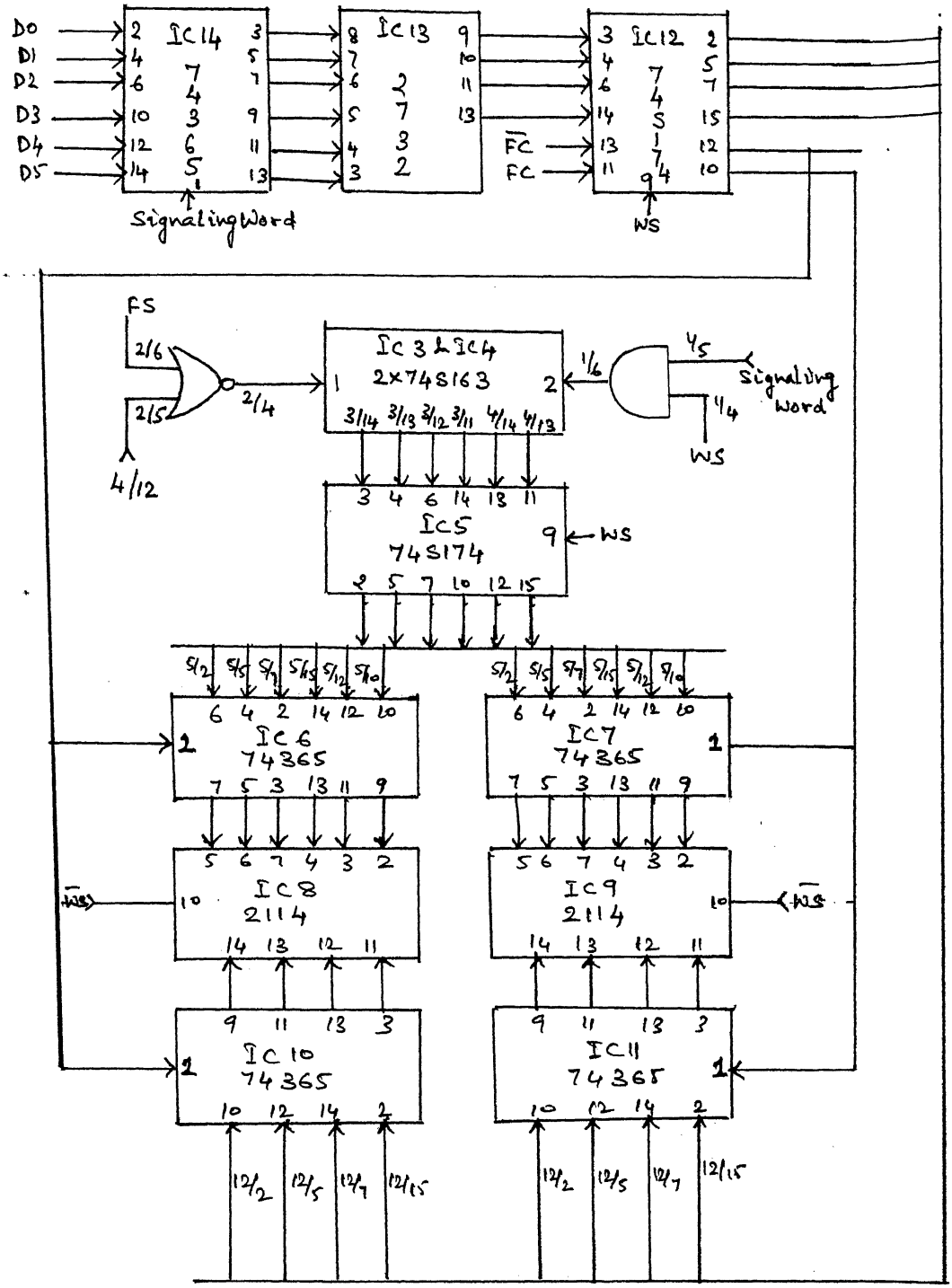


FIG. 4.6 : CIRCUIT DIAGRAM OF THE DECODER

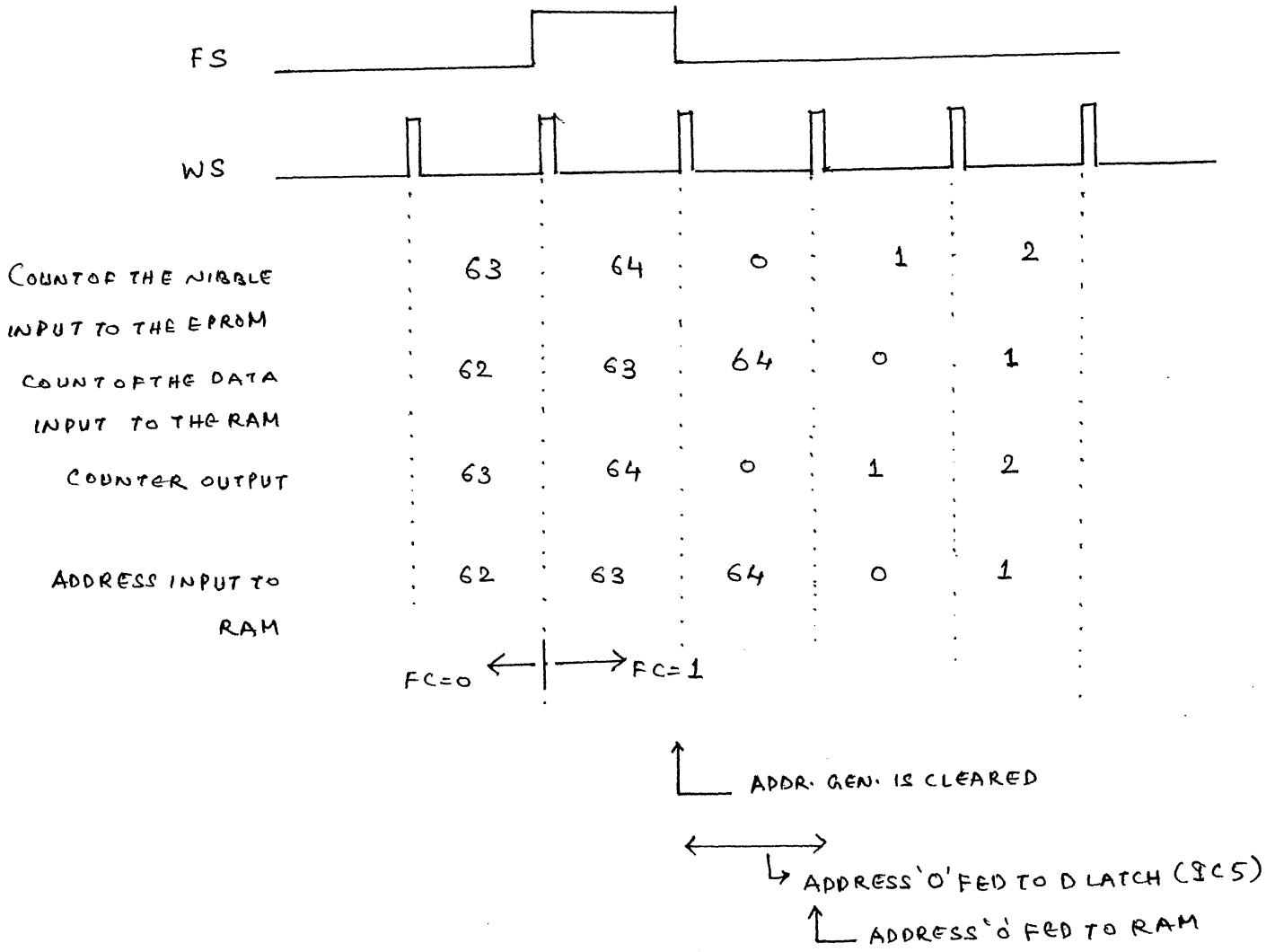


FIG. 4.7 : TIMING DIAGRAM OF THE DECODER

Address A5-A0	Data D3-D0	Address A5-A0	Data D3-D0
000000	1111	100000	1111
000001	1111	100001	1111
000010	1111	100010	1111
000011	1111	100011	1111
000100	1111	100100	0010
000101	1111	100101	1000
000110	1111	100110	0001
000111	1111	100111	1111
001000	1111	101000	1111
001001	1111	101001	1001
001010	1101	101010	1010
001011	1011	101011	1111
001100	1111	101100	1110
001101	1111	101101	1111
001110	1111	101110	1111
001111	1111	101111	1111
010000	1111	110000	1111
010001	1111	110001	1111
010010	1111	110010	0000
010011	0110	110011	1111
010100	1111	110100	0011
010101	0101	110101	0010
010110	0100	110110	1111
010111	1111	110111	1111
011000	1111	111000	1111
011001	1100	111001	1111
011010	0111	111010	1111
011011	1101	111011	1111
011100	1111	111100	1111
011101	1111	111101	1111
011110	1111	111110	1111
011111	1111	111111	1111

TABLE 4.3 : Decoder EPROM Contents

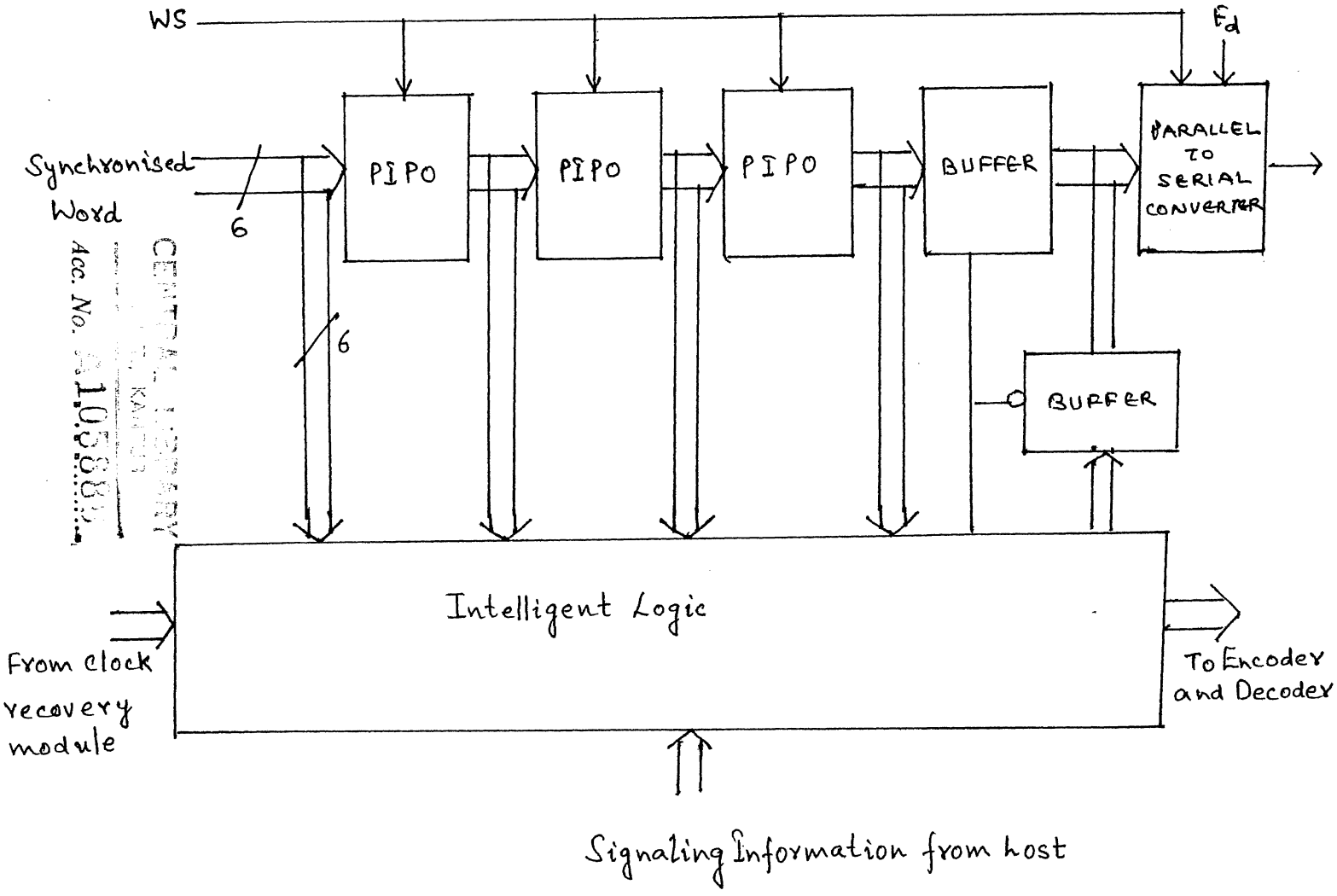


FIG. 4.8 : BLOCK SCHEMATIC OF THE SIGNALING PROCESSOR

and IC9). The address and data buffers of a RAM are enabled when the RAM is in the write mode. LE signal is used as a write pulse. During an odd frame if data is being written into a RAM it would be read out in the even frame nibble by nibble. At the same time data would be written into the other RAM in the even frame and read out during the odd frame. This is done by using FC and FC signal to enable the buffers. The timing diagram of the decoder is given in Fig.4.7.

4.4 SIGNALING PROCESSOR (PROPOSED)

The schematic of the proposed signaling processor is shown in Fig.4.8. The data is delayed by 24 bits using the Parallel In Parallel Out (PIPO) registers which are clocked by WS. The logic circuit on receiving a request for a slot from the host, examines the signaling slot and sets the reservation bits using its register and the multiplexer. Addressing can also be done in a similar fashion. This circuit has not been developed.

4.5 CONCLUSION :

In this chapter the details of implementation of the clock recovery and synchronization circuit, the encoder and the decoder has been discussed in detail. A schematic for the signaling processor has been proposed. In the present work, for testing purposes the LSB of the slot counter output has been used to statically assign slots to the node.

CHAPTER 5

CONCLUSIONS

5.1 SUMMARY OF THE WORK

The design of a 16 Mbps synchronous TDMA ring network which carries 8 slots per frame and can support voice and data traffic has been carried out. The feasibility of the network has been partially demonstrated by implementing a scaled down version of the network. The design of the node is modular and the nodes require similar hardware.

The network provides the nodes with access to 2.048 Mbps slots. The nodes can thus provide users with primary ISDN access. The bandwidth is also sufficient to support 30 multiplexed voice channels.

5.2 SUGGESTIONS FOR FURTHER WORK

(1) The use of faster RAMs for switching and PROMs for the encoder and decoder can increase the speed of the network considerably with the same architecture.

(2) The interface of the host to the node has to be designed.

(3) The ring controller has to be designed which can do the system monitoring and provide toll information using the presently unassigned bits of the signalling slot.

(4) The fault detector circuit and the node bypass circuitry are to be developed to improve the reliability of the network.

(5) A study of the throughput and delay characteristics of the network for different loads can be carried out.

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